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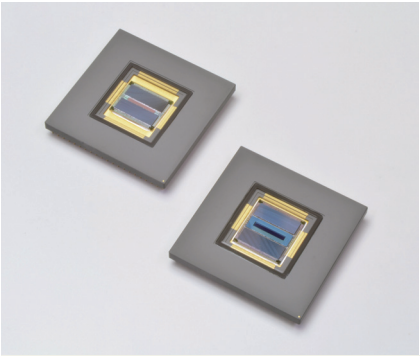
TDI-CCD image sensors



S14810 S14813

Hybrid structure combining TDI-CCD and CMOS readout circuit

These image sensors combine a TDI-CCD, which can ensure adequate brightness for images even during high speed imaging, with a CMOS readout circuit for digital output. The S14813 (back-thinned type) has higher sensitivity than the S14810 (front-illuminated type) in the ultraviolet to visible region, ensuring clear images even at low illuminance.

Features

- **Sensors combining TDI-CCD and CMOS readout circuit**
- **Effective bit number: 9.4-bit (data width: 10-bit)**
- **High-speed line rate: 100 kHz max.**
- **High UV resistance (S14813)**
- **Low noise: 12 e^- rms typ. (S14813)**
  8 e^- rms typ. (S14810)
- **Bidirectional transfer**

Applications

- **Continuous imaging of high-speed moving objects**
- **Machine vision**

Structure

Parameter		Specification
Pixel size (H × V)		12 × 12 µm
Total number of pixels (H × V)		1024 × 132
Number of effective pixels (H × V)		1024 × 128
Image size (H × V)		12.288 × 1.536 mm
Fill factor		100%
Number of TDI stages		128
Anti-blooming		FW × 100 min.
Vertical clock		2-phase (bidirectional)
Output circuit		10-bit A/D converter
Package		320-pin ceramic (see dimensional outlines)
Window material	S14810	Borosilicate glass*1
	S14813	Quartz glass*1
Cooling		Non-cooled

*1: Resin sealing

Note: This product is not hermetically sealed, and therefore moisture may penetrate into the package. Storing or using the product in a place with sudden temperature or humidity changes may cause condensation to form inside the package, so avoid such environments.

Absolute maximum ratings (Ta=25 °C unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Operating temperature*2		Topr	0	-	60	°C
Storage temperature		Tstr	-40	-	70	°C
Output transistor drain voltage		VOD	-10	-	9.5	V
Reset drain voltage		VRD	-10	-	7.5	V
Overflow drain voltage		VOFD	-10	-	7.5	V
Overflow gate voltage		VOFG	-20.5	-	7.5	V
Summing gate voltage		VSG	-20.5	-	4.5	V
Reset gate voltage		VRG	-20.5	-	4.5	V
Output gate voltage		VOG	-20.5	-	4.5	V
Vertical clock voltage		VPXV	-20.5	-	4.5	V
CCD ground voltage		VAGND	-11.5	-	-9.5	V
ROIC supply voltage	Analog terminal	Vdd(A)	-0.3	-	3.9	V
	Digital terminal	Vdd(D)	-0.3	-	3.9	
	Counter terminal	Vdd(C)	-0.3	-	3.9	
ROIC digital input terminal voltage*3		Vi	-0.3	-	3.9	V
Soldering conditions*4		Tsol	260 °C, within 5 s, at least 2 mm away from lead roots			-

*2: Package temperature
*3: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, CLK, TG_reset, PLL_reset
*4: Use a soldering iron.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating condition (TDI mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		VOD	2.5	4.5	6.5	V
Reset drain voltage	S14810	VRD	-0.5	1.5	3.5	V
	S14813		-1.5	0.5	2.5	
Overflow drain voltage		VOFD	-0.5	1.5	3.5	V
Overflow gate voltage		VOFG	-7.5	-5.5	-3.5	V
Output gate voltage		VOG	-7.5	-5.5	-3.5	V
Summing gate voltage		VSGH	-5.5	-3.5	-1.5	V
		VSGL	-15.5	-13.5	-11.5	
Reset gate voltage		VRGH	-3.5	-1.5	0.5	V
		VRGL	-13.5	-11.5	-9.5	
Vertical clock voltage		VPXVH	-5.5	-3.5	-1.5	V
		VPXVL	-15.5	-13.5	-11.5	
CCD ground voltage		VAGND	-	-10.5	-	V
ROIC supply voltage	Analog terminal	Vdd(A)	3.2	3.3	3.45	V
	Digital terminal	Vdd(D)	3.2	Vdd(A)	3.45	
	Counter terminal	Vdd(C)	2.6	2.7	2.9	
ROIC digital input terminal voltage*5		VIH	Vdd(D) - 0.25	Vdd(D)	Vdd(D) + 0.25	V
		VIL	0	-	0.25	

*5: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, CLK, TG_reset, PLL_reset

Electrical characteristics

Digital input

[Ta=25 °C, Typ. values in operating conditions table (P.2), unless otherwise noted]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Master clock pulse frequency		f(CLK)	25	30	35	MHz
Master clock pulse duty ratio		D(CLK)	45	50	55	%
Digital input signal	Rise time*6 *7	tr(sigi)	-	5	7	ns
	Fall time*6 *7	tf(sigi)	-	5	7	

*6: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, CLK, TG_reset, PLL_reset
*7: Time for the input voltage to rise or fall between 10% and 90%

Digital output

[Ta=25 °C, Typ. values in operating conditions table (P.2), unless otherwise noted]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Data rate		DR		f(CLK) × 8		MHz
Pixel sync signal (PCLK) frequency		f(PCLK)		f(CLK) × 4		MHz
Digital output voltage (LVDS output)	Offset	Vofs	1.13	1.25	1.38	V
	Differential	Vdiff	0.25	0.35	0.45	V
	Rise time*8 *9	tr(out)	-	2	3	ns
	Fall time*8 *9	tf(out)	-	2	3	ns

*8: Out_A to H, Vsync, Hsync, PCLK, CTR
*9: Time for the output voltage to rise or fall between 10% and 90% when there is a 2 pF load capacitor attached to the output terminal

CCD

[Ta=25 °C, Typ. values in operating conditions table (P.2), unless otherwise noted]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Line rate	LR	-	100	100	kHz
Vertical shift register capacitance	C_{PXV}	-	1200	-	pF
Summing gate capacitance	C_{SG}	-	40	-	pF
Reset gate capacitance	C_{RG}	-	40	-	pF
Charge transfer efficiency	CTE	0.99995	0.99999	-	-

Current consumption

Parameter		Symbol	S14810			S14813			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption	Analog and digital terminal*10	I1	-	430	600	-	430	600	mA
	Counter terminal*11	I2	-	250	350	-	230	350	

*10: Total value of 2 ROICs
*11: Saturated

A/D converter

Parameter		Symbol	Specification	Unit
Resolution		RESO	10	bit
A/D resolution	High*12	-	0.17	mV/DN
	Low*13	-	1.67	

*12: Gain=10x
*13: Gain=1x

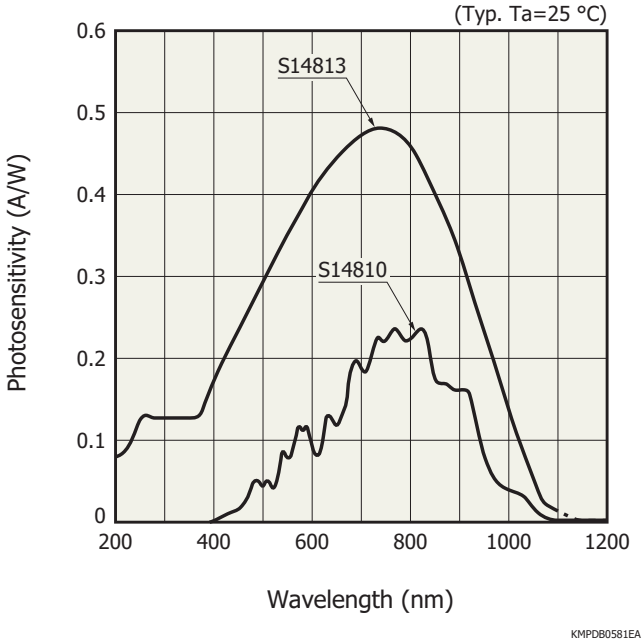
Electrical and optical characteristics

[Ta=25 °C, Typ. values in operating conditions table (P.2), unless otherwise noted]

Parameter		Symbol	S14810			S14813			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Spectral response range		λ		400 to 1100			200 to 1100		nm
Conversion efficiency	Low*14	-	-	25	-	-	15	-	μV/e⁻
	Low*14		-	0.015	-	-	0.009	-	DN/e⁻
	High*15		-	250	-	-	150	-	μV/e⁻
	High*15		-	0.15	-	-	0.09	-	DN/e⁻
Saturation output*16	Low*14	Vsat	600	675	-	585	675	-	DN
	High*15		600	675	-	480	550	-	
Full well capacity*17	Low*14	FW	40	45	-	65	75	-	ke⁻
	High*15		4	4.5	-	5.3	6.1	-	
Saturation output voltage		Vsat	-	FW × Sv	-	-	FW × Sv	-	V
Photoresponse nonuniformity*18		PRNU	-	±3	±10	-	±3	±10	%
Dark current*19		DS	-	10	15	-	10	15	ke⁻/pixel/s
Dark output	Low*14	DSD	-	150	-	-	90	-	DN/s
	High*15		-	1500	-	-	900	-	
Readout noise	Low*14	Nread	-	30	50	-	40	80	e⁻ rms
	High*15		-	8	15	-	12	20	
Random noise	Low*14	RN	-	0.45	0.75	-	0.36	0.72	DN rms
	High*15		-	1.2	2.25	-	1.08	1.80	
Dynamic range*20	Low*14	Drange	800	1500	-	813	1875	-	-
	High*15		267	563	-	267	509	-	
	*21		2670	5630	-	3250	6250	-	
Offset output*22	Low*14	Vo	0	200	300	0	210	300	DN
	High*15		0	200	300	0	320	400	
Offset variation*23	Low*14	DSNU	-	3	10	-	3	10	DN rms
	High*15		-	3	15	-	7	15	

*14: Gain=1x
*15: Gain=10x
*16: Maximum output, where linearity is ±5% or smaller while the offset output is subtracted
*17: Electron charge corresponding to saturation output
*18: PRNU=ΔX/X × 100 [%]
ΔX: standard deviation of all effective pixel output, X: average output of all effective pixels
*19: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*20: Ratio between saturation charge and readout noise
*21: Total where gain is 1x and 10x
*22: Average output value of all effective pixels under light-shielded condition
*23: Standard deviation of output values of all effective pixels under light-shielded condition
Note: DN (digital number): unit of A/D converter output

Spectral response (with window)



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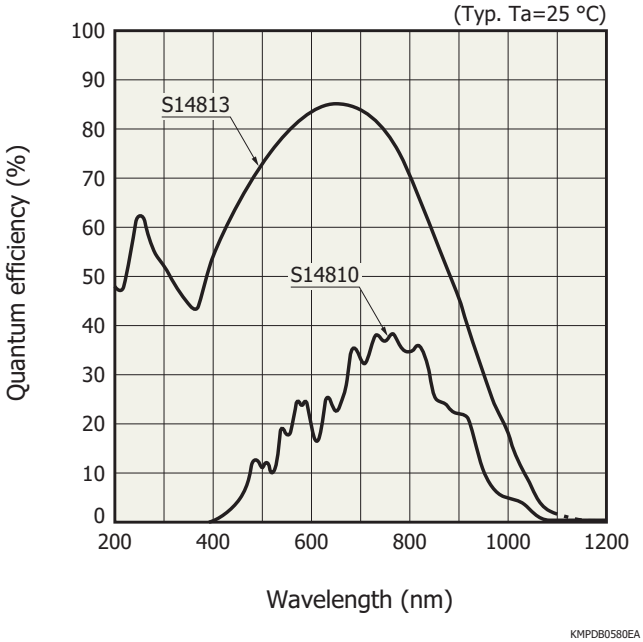

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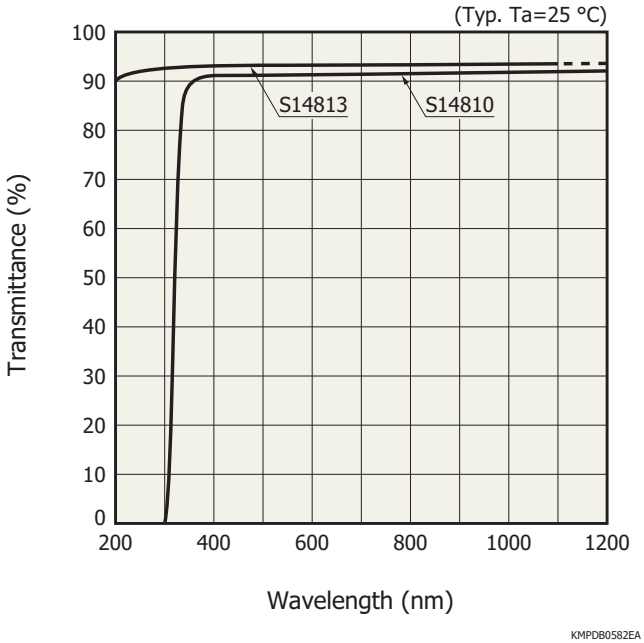
Spectral transmittance of window material



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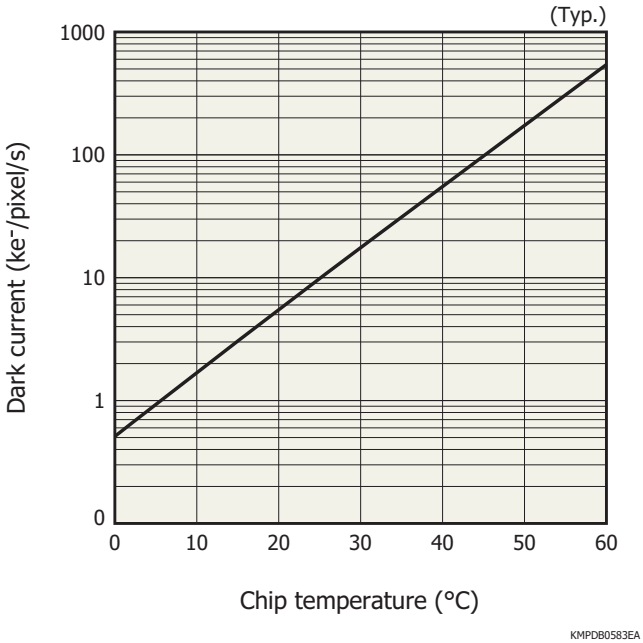
Dark current vs. chip temperature



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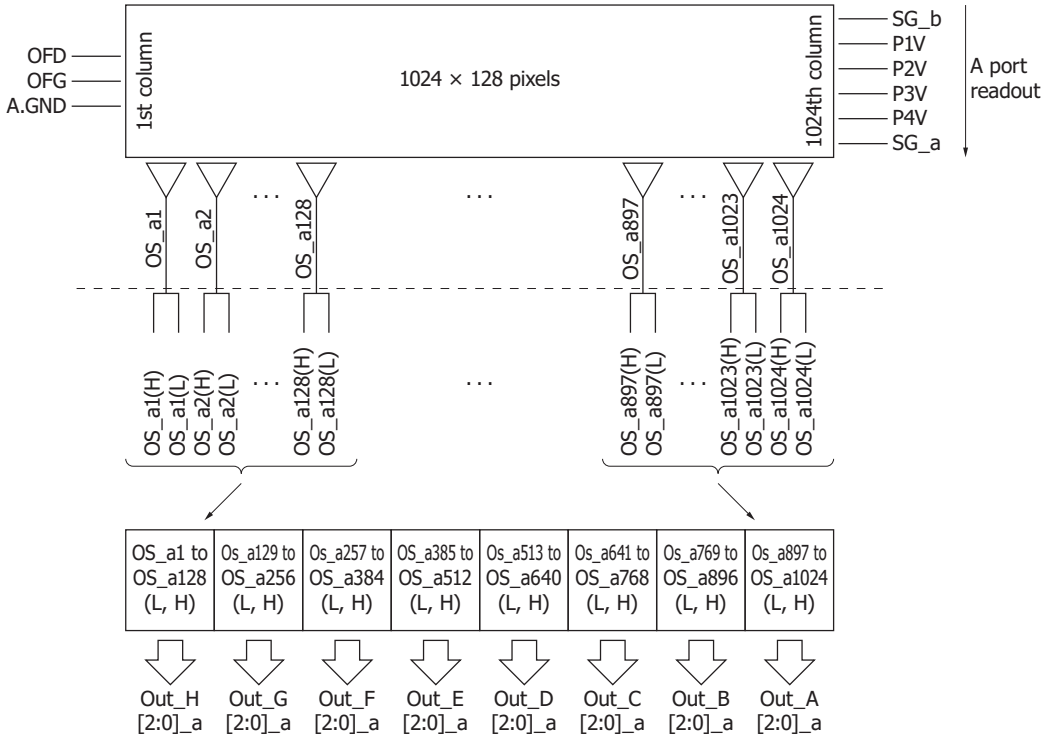
Sensor structure

A port



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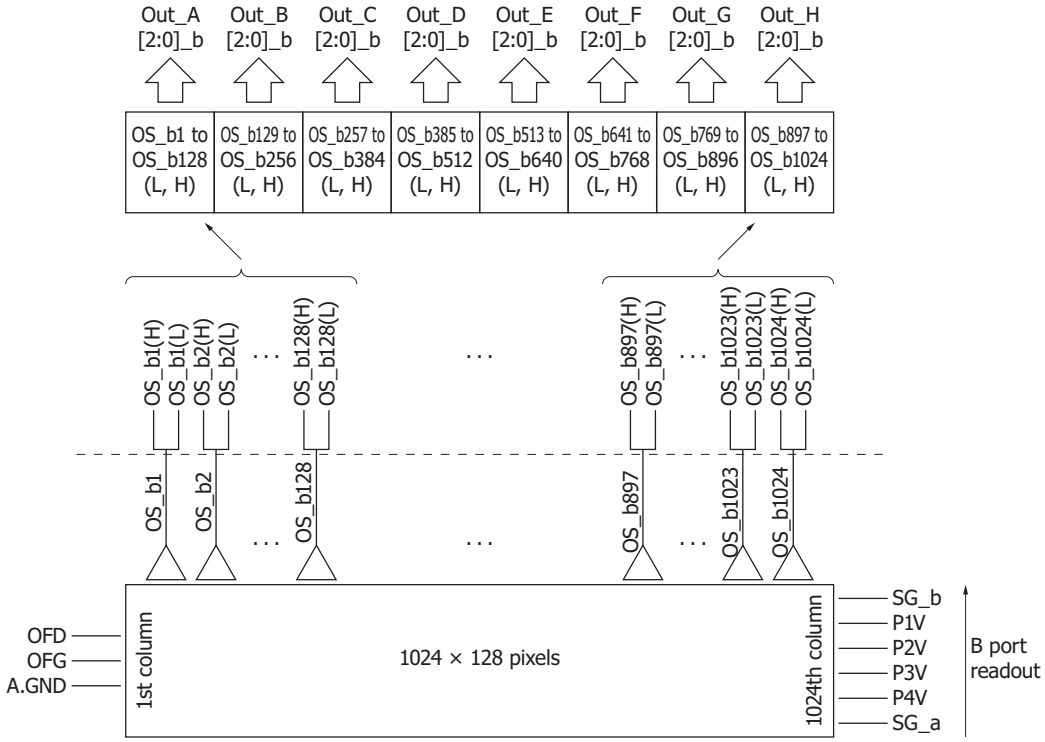
B port



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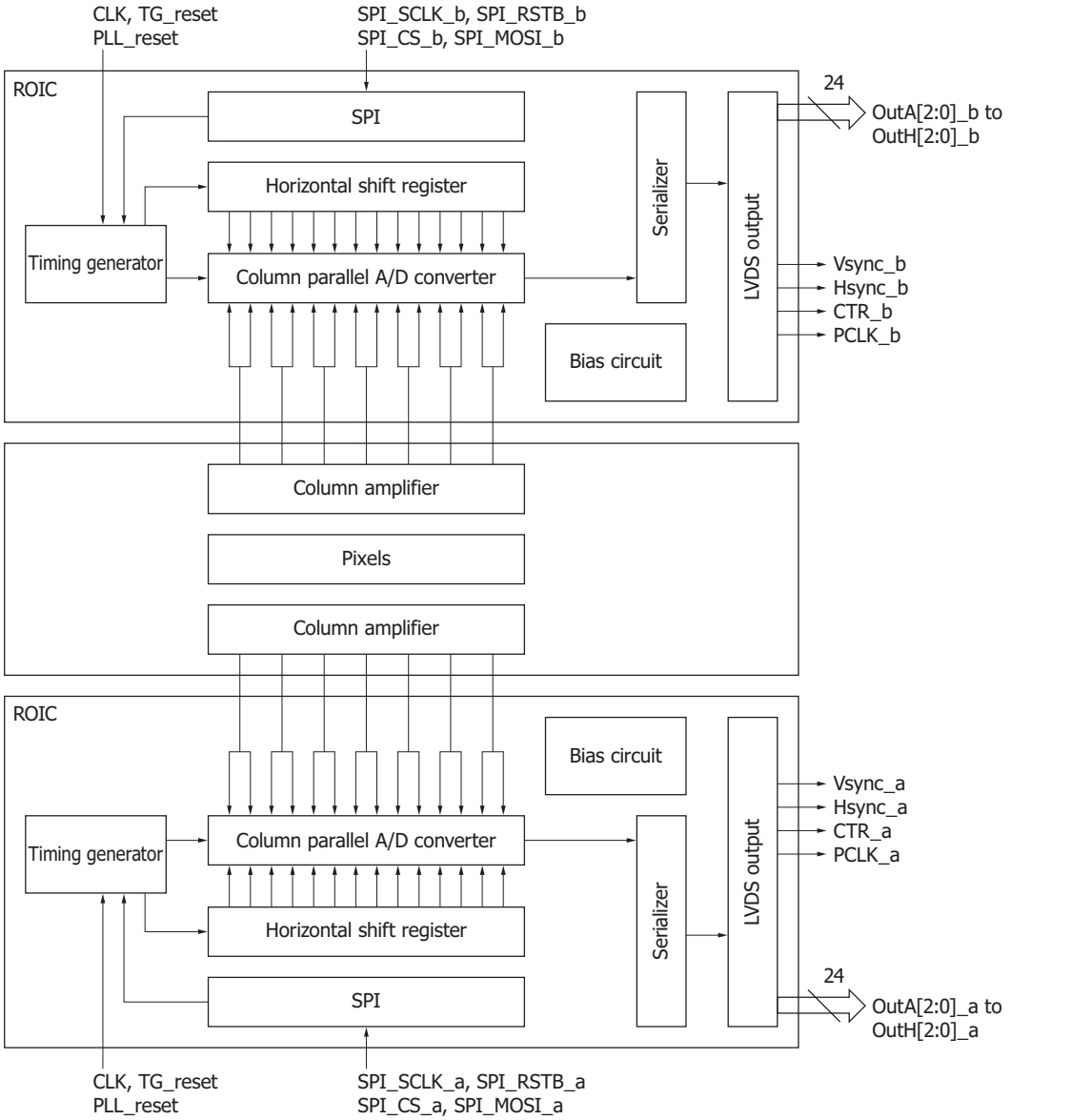
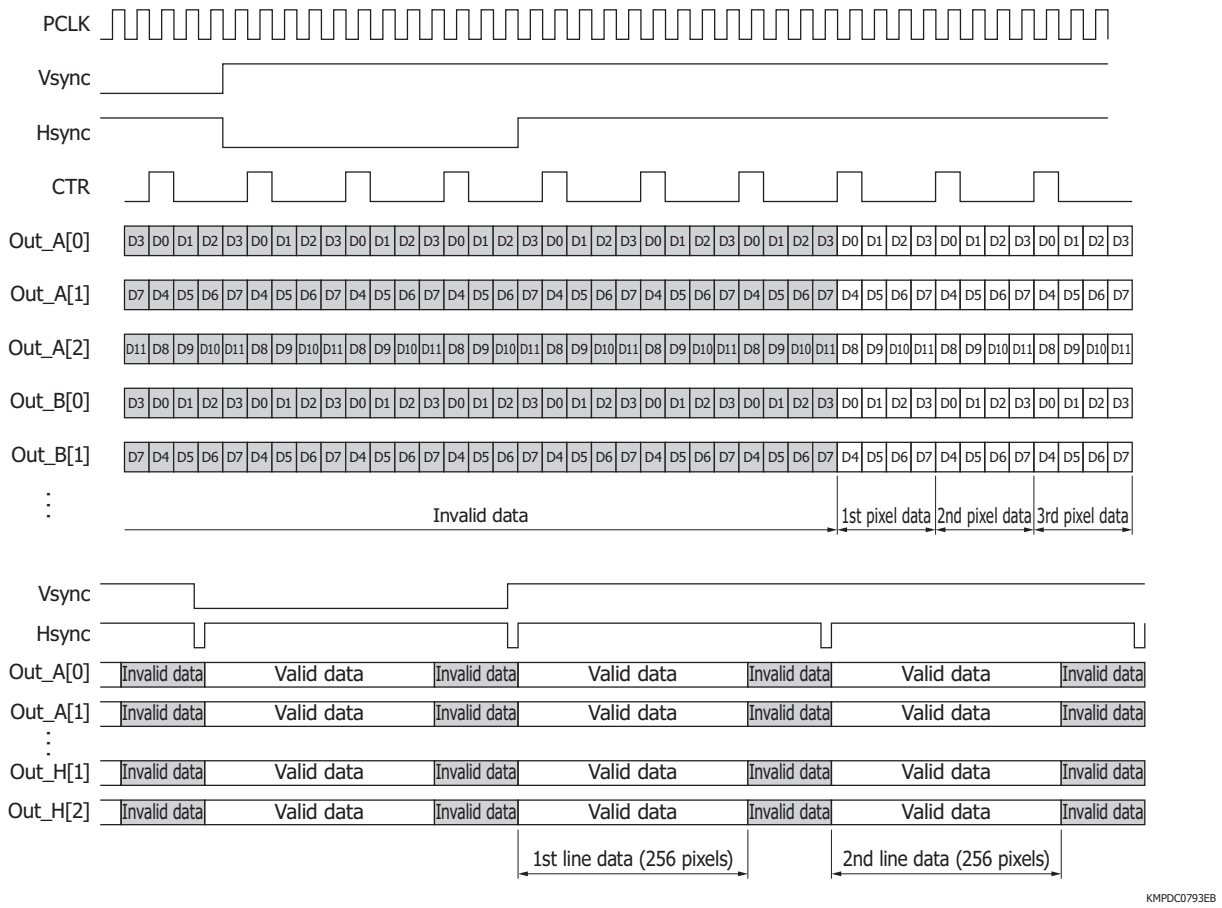
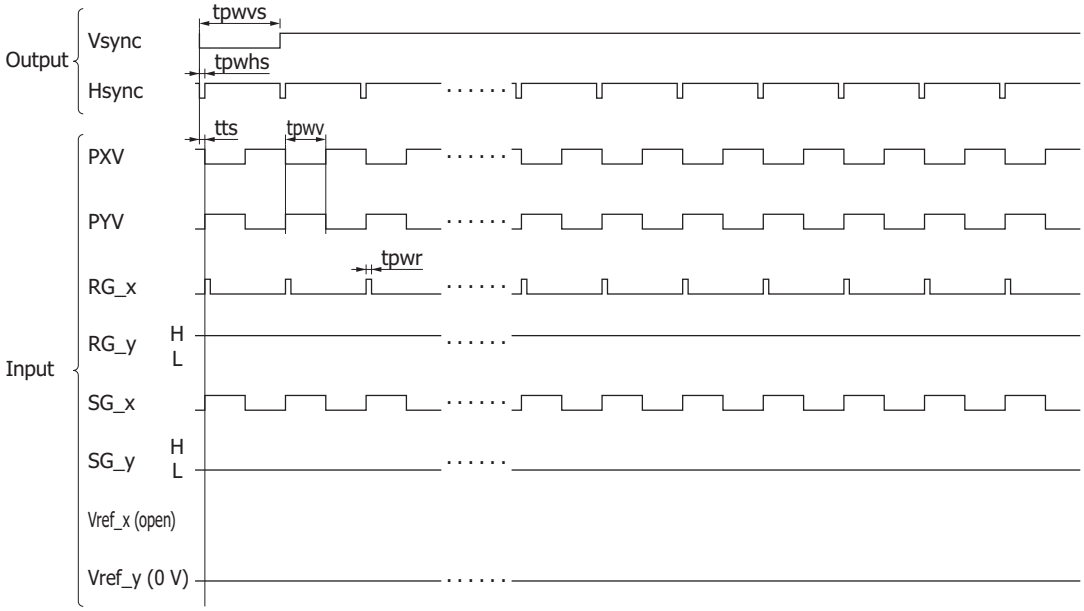
Block diagram



Timing chart



TDI mode



KMPDC0794EB

■ Vertical clock phase

Readout port	PXV	PYV
A	P1V, P2V	P3V, P4V
B	P2V, P3V	P1V, P4V

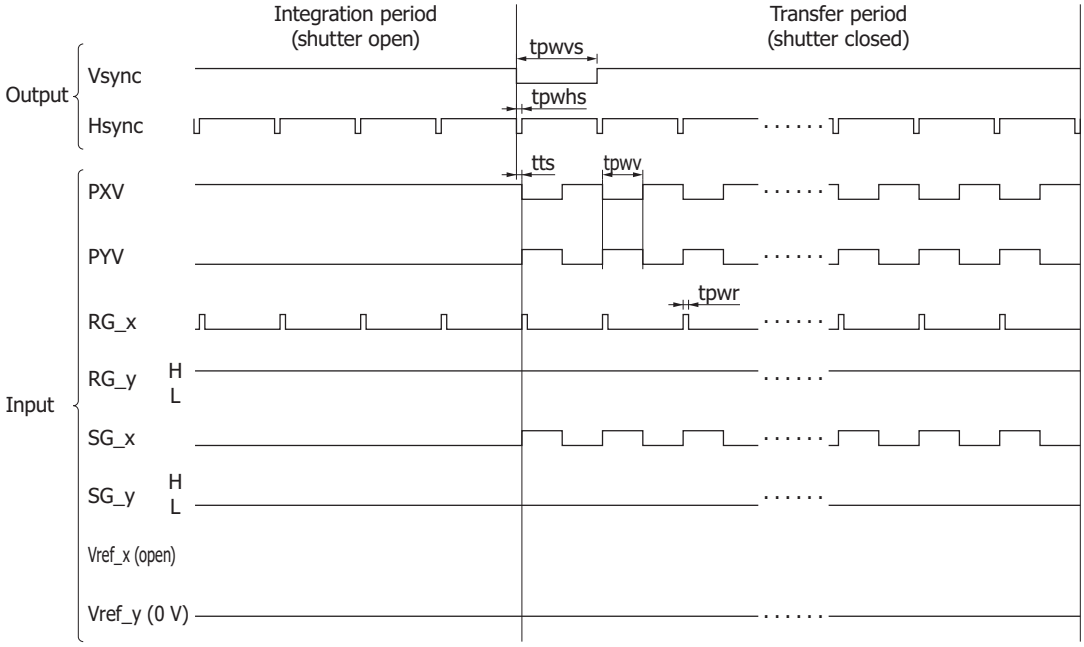
■ RG, SG, Vref

Readout port	RG_x	RG_y	SG_x	SG_y	Vref_x	Vref_y
A	RG_a	RG_b	SG_a	SG_b	Vref1_a, Vref3_a	Vref1_b, Vref3_b
B	RG_b	RG_a	SG_b	SG_a	Vref1_b, Vref3_b	Vref1_a, Vref3_a

■ ADC_N [7:0], DO_N [7:0]

Readout port	A port SPI	B port SPI
A	0	199
B	199	0

Area scanning mode



KMPDC0795EB

■ Vertical clock phase

Readout port	PXV	PYV
A	P1V, P2V	P3V, P4V
B	P2V, P3V	P1V, P4V

■ RG, SG, Vref

Readout port	RG_x	RG_y	SG_x	SG_y	Vref_x	Vref_y
A	RG_a	RG_b	SG_a	SG_b	Vref1_a, Vref3_a	Vref1_b, Vref3_b
B	RG_b	RG_a	SG_b	SG_a	Vref1_b, Vref3_b	Vref1_a, Vref3_a

■ ADC_N [7:0], DO_N [7:0]

Readout port	A port SPI	B port SPI
A	0	199
B	199	0

Parameter		Symbol	Min.	Typ.	Max.	Unit
PXV, PYV*24 SG*24	Pulse width	tpwv	-	5	-	µs
	Rise and fall times	tprv, tpfv	10	-	-	ns
	Duty ratio	-	-	50	-	%
RG	Pulse width	tpwr	500	600		ns
	Rise and fall times	tprr, tpfr	5	-	-	ns
Vsync-CCD clock timing shift		tts	-100	0	100	ns

*24: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

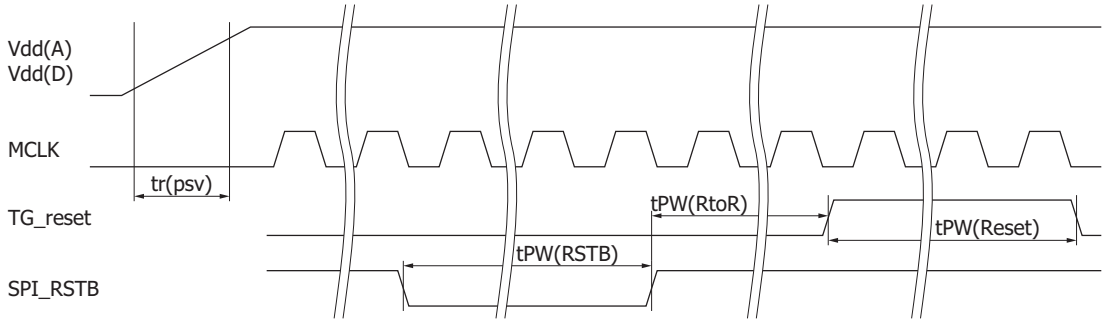
Parameter		Symbol	Min.	Typ.	Max.	Unit
Vsync	Pulse width*25	tpwvs	-	300	-	cycles
Hsync	Pulse width*25	tpwhs	-	3	-	cycles

*25: One cycle is the period of a single master clock cycle.

Digital output timing

Reset input at power-on

Raise all the supply voltage to meet the operating conditions, then input "Tg_reset" and "SPI_RSTB" as shown below to initialize the timing generator and the SPI circuit.



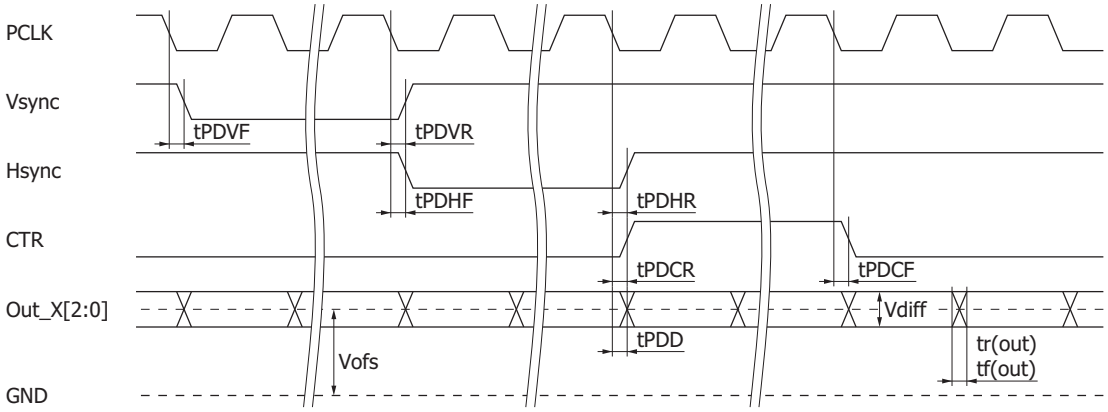
KMPDC0796EA

[Ta=25 °C, Typ. values in operating conditions in table (P.2), unless otherwise noted]

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI_RSTB signal low period at power-on	tPW(RSTB)	100	-	-	ns
Interval between SPI_RSTB signal and TG_Reset signal at power-on	tPW(RtoR)	100	-	-	ns
TG_Reset signal high period at power-on*26 *27	tPW(Reset)	3	-	-	cycles
Supply voltage rise time*28	tr(psv)	-	20	-	ms

*26: Incorrect data is output in the first frame after the reset signal is input. Use the data in the second frame or later.
*27: One cycle is the period of a single master clock cycle.
*28: The time period where the supply voltage is increased from 10% to 90% with 1 µF external load capacitor, during the power-on time or readout direction switch time

Digital output (LVDS)



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Parameter		Symbol	Min.	Typ.	Max.	Unit
Data rate (per port)		VR		f(CLK)		Hz
Digital output voltage (LVDS output)	Offset	Vofs	1.13	1.25	1.38	V
	Differential	Vdiff	0.25	0.35	0.45	V
Digital output signal	Rise time*29 *30	tr(out)	-	2	3	ns
	Fall time*29 *30	tf(out)	-	2	3	
PCLK - Dout delay time		tPDD	-	-	3	ns
PCLK - Hsync delay time	Rise time	tPDHR	-	-	5	ns
	Fall time	tPDHF	-	-	5	
PCLK - Vsync delay time	Rise time	tPDVR	-	-	5	ns
	Fall time	tPDVF	-	-	5	
PCLK - CTR delay time	Rise time	tPDCR	-	-	3	ns
	Fall time	tPDCF	-	-	3	

*29: Dout, Vsync, Hsync, PCLK, CTR
*30: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor attached to the output terminal

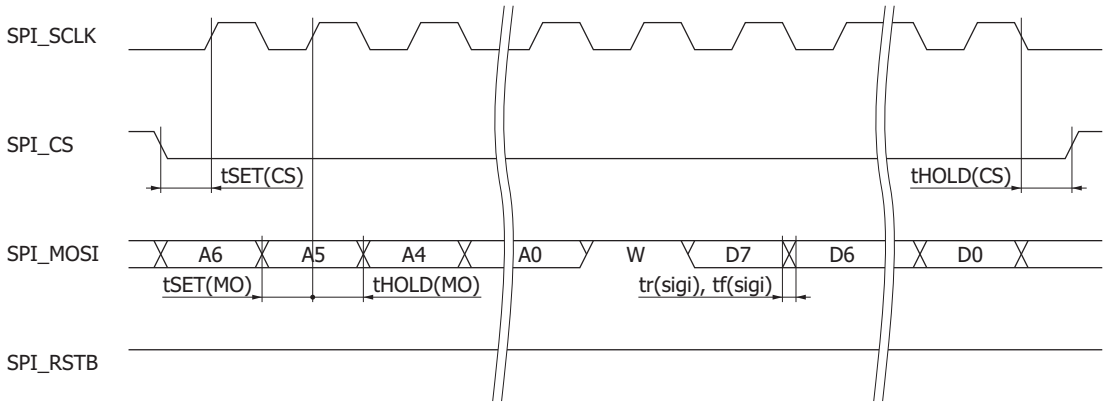
SPI

Following parameters can be selected in SPI (serial peripheral interface).

· Offset adjustment of analog amplifier output
· Operation mode setting of A/D converter

Set the SPI using SPI_SCLK, SPI_CS, SPI_MOSI, and SPI_RSTB.
SPI_SCLK : SPI clock signal
SPI_CS : SPI selection signal
SPI_MOSI: SPI input signal
SPI_RSTB: SPI reset signal

SPI input

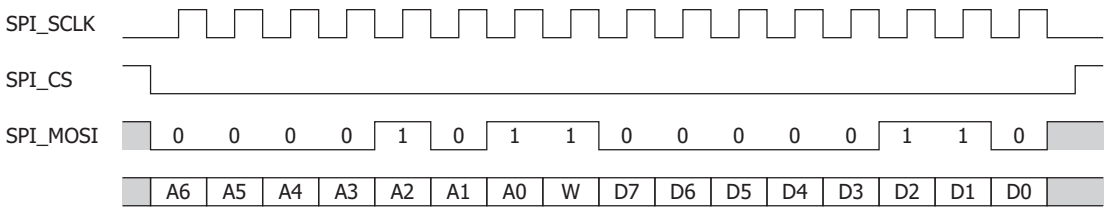


KMPDC0799EA

Parameter		Symbol	Min.	Typ.	Max.	Unit
SPI clock pulse frequency		f(SCLK)	-	-	10	MHz
SPI setup time (SPI_CS)		tSET(CS)	7	-	-	ns
SPI hold time (SPI_CS)		tHOLD(CS)	7	-	-	ns
SPI setup time (SPI_MOSI)		tSET(MO)	7	-	-	ns
SPI hold time (SPI_MOSI)		tHOLD(MO)	7	-	-	ns
Digital input signal	Rise time*31	tr(sigi)	-	5	7	ns
	Fall time*31	tf(sigi)	-	5	7	

*31: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor attached to the output terminal

SPI address setting



KMPDC0800EA

Address	Name	Initial value		Recommended value				Description
		S14810, S14813		S14810		S14813		
		Binary system	Decimal system	Binary system	Decimal system	Binary system	Decimal system	
0	-	-000 0000	0	-010 0001	33	-010 0001	33	Fixed value (Set to recommended value)
1	MODE2[2:0]	---- -000	0	---- -000	0	---- -000	0	Mode2[0]=0: normal mode Mode2[0]=1: dummy pattern output mode Mode2[2]=0: normal mode Mode2[2]=1: LVDS current cut mode Refer to P.15 for the dummy pattern output example. (Do not change the setting for other bits)
2	-	---- ----	-	---- ----	-	---- ----	-	Not used (Do not change the settings)
3	-	---- ----	-	---- ----	-	---- ----	-	
4	-	---- ----	-	---- ----	-	---- ----	-	
5	CntEnd[7:0]	0110 0000	96	0110 0010	98	0110 0010	98	See the line rate settings (P.15).
6	-	---- ----	-	---- ----	-	---- ----	-	Not used (Do not change the settings)
7	-	---- ----	-	---- ----	-	---- ----	-	
8	-	---- ----	-	---- ----	-	---- ----	-	
9	-	---- ----	-	---- ----	-	---- ----	-	
10	-	---- ----	-	---- ----	-	---- ----	-	
11	-	---- ----	-	---- ----	-	---- ----	-	
12	-	---- ----	-	---- ----	-	---- ----	-	
13	WinWV[15:8]	0000 0100	1040	0000 0001	300	0000 0001	300	The number of readout rows are set in WinWV[15:0].
14	WinWV[7:0]	0001 0000		0010 1100		0010 1100		
15	-	---- ----	-	---- ----	-	---- ----	-	Not used (Do not change the settings)
16	-	---- ----	-	---- ----	-	---- ----	-	
17	-	---- ----	-	---- ----	-	---- ----	-	
18	-	---- ----	-	---- ----	-	---- ----	-	
19	-	---- ----	-	---- ----	-	---- ----	-	
20	-	---- 0011	3	---- 1100	12	---- 1100	12	Fixed value (Set to recommended value)
21	-	---- ----	-	---- ----	-	---- ----	-	Not used (Do not change the settings)
22	-	---- ----	-	---- ----	-	---- ----	-	
23	-	0000 0110	6	0000 0111	7	0000 0111	7	Fixed value (Set to recommended value)
24	ADC_N[7:0]	0000 0000	0	0000 0000	0	0000 0000	0	*32
25	-	0000 0110	6	0000 0011	3	0000 0011	3	Fixed value (Set to recommended value)
26	DO_N[7:0]	0000 0000	0	0000 0000	0	0000 0000	0	*32
27	-	0000 0001	1	0000 0011	3	0000 0011	3	Fixed value (Set to recommended value)
28	-	0000 0011	3	0000 0010	2	0000 0010	2	
29	-	---- ----	-	---- ----	-	---- ----	-	Not used (Do not change the settings)
30	TG_N[7:0]	0001 0011	19	0000 0010	2	0000 0010	2	See the line rate settings (P.15).
31	-	0000 0100	4	0000 1101	13	0001 0010	18	Fixed value (Set to recommended value)
32	-	0001 0000	16	0001 0100	20	0001 1000	24	
33	-	0001 0000	16	0001 0100	20	0001 1000	24	
34	-	0010 1000	40	0010 0100	36	0010 0100	36	
35	-	---- ----	-	---- ----	-	---- ----	-	Not used (Do not change the settings)
36	-	---- ----	-	---- ----	-	---- ----	-	
37	-	---- ----	-	---- ----	-	---- ----	-	
38	-	---- ----	-	---- ----	-	---- ----	-	
39	-	0010 0000	32	0001 0100	20	0001 0100	20	Fixed value (Set to recommended value)
40	-	0001 1000	24	0001 1100	28	0001 1100	28	
41	-	0001 0000	16	0001 1011	27	0001 1011	27	
42	-	0000 0000	0	0000 1110	14	0000 1110	14	
43	-	0000 1000	8	0000 0000	0	0000 0000	0	
44	-	0000 1010	10	0001 0100	20	0001 0100	20	
45	-	---- ----	-	---- ----		---- ----	-	Not used (Do not change the settings)
46	-	---- ----	-	---- ----		---- ----	-	
47	-	---- 0000	64	---- 0000	200	---- 0000	200	Fixed value (Set to recommended value)
48	-	0100 0000		1100 1000		1100 1000		
49	-	---- ----	-	1100 1000	200	1100 1000	200	

*32: Change the readout/halt state of ROIC in ADC_N [7:0] and DO_N [7:0] (readout setting value: 0, halt state setting value: 199).

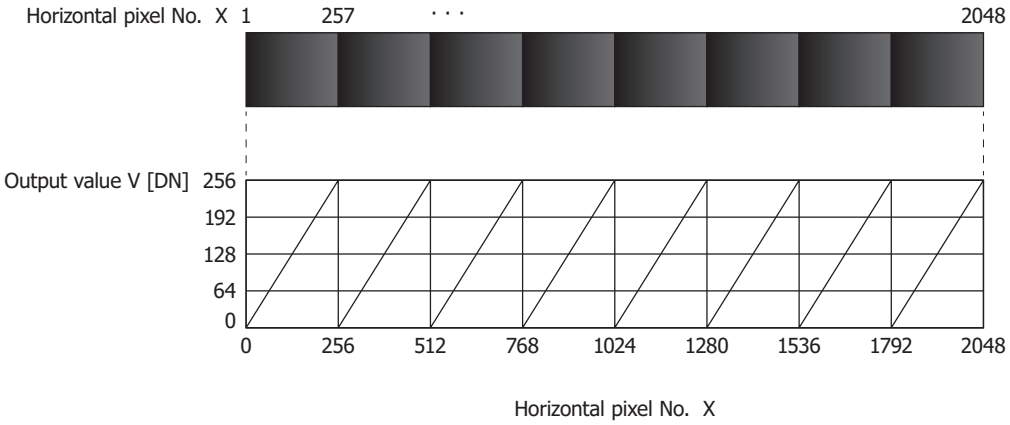
Line rate settings

TG_N	CntEnd	Line rate LR (kL/s)	tpwv (µs)
2	98	100.0	5.0
5	77	50.0	10.0
8	70	33.3	15.0
11	67	25.0	20.0
14	65	20.0	25.0

Note: Line rate settings other than specified above are not recommended.

$$LR = \frac{f(CLK)}{100\ (TG\_N + 1)}\ [Hz]$$

Dummy pattern output example



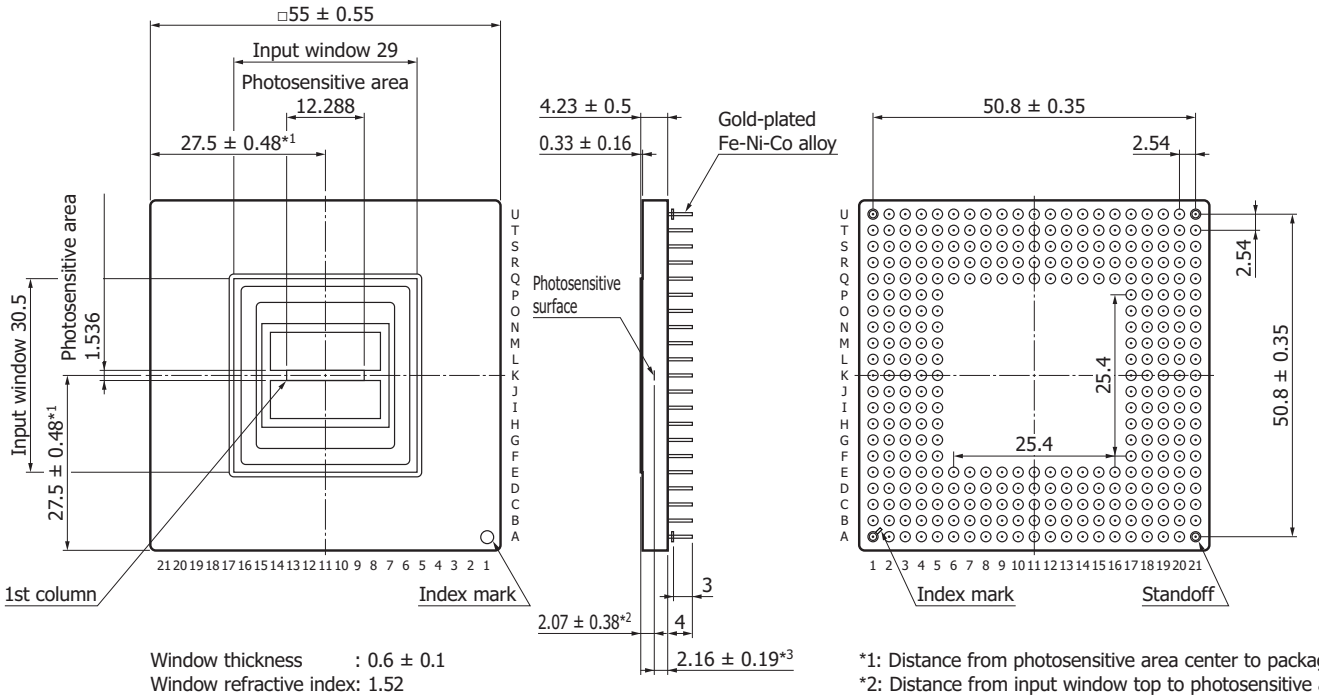
KMPDC0953EA

	X: Horizontal pixel No.																		
	1	2	3	·	·	253	254	255	256	257	·	·	·	·	·	·	·	2047	2048
Output value V *33[DN]	2	3	4	·	·	254	255	0	1	2	·	·	·	·	·	·	·	0	1

*33: Output value V of the dummy pattern is defined as follows with horizontal pixel No. X being a variable.
V=mod (X + 1, 256)

Dimensional outlines (unit: mm)

S14810

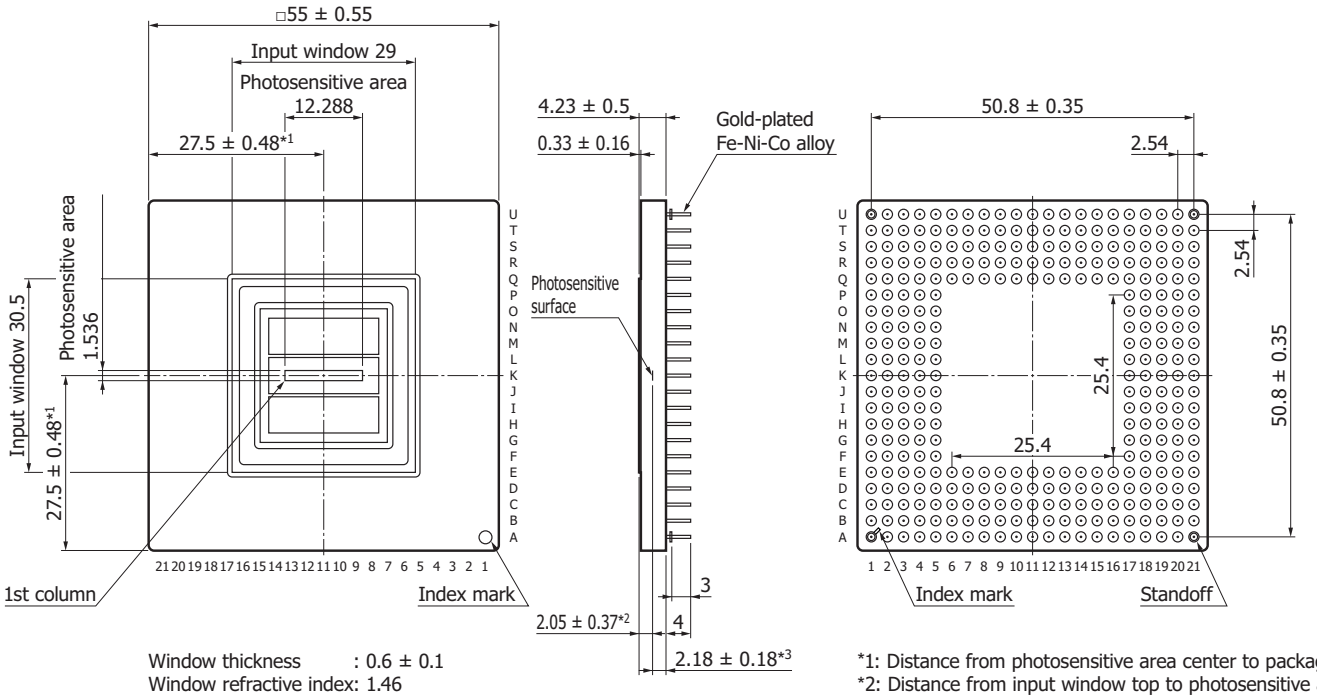


Window thickness : 0.6 ± 0.1
Window refractive index: 1.52
Weight : 40 g
AR coating : none

*1: Distance from photosensitive area center to package edge
*2: Distance from input window top to photosensitive area
*3: Distance from package bottom to photosensitive surface

KMPDA0625EB

S14813



Window thickness : 0.6 ± 0.1
Window refractive index: 1.46
Weight : 40 g
AR coating : none

*1: Distance from photosensitive area center to package edge
*2: Distance from input window top to photosensitive area
*3: Distance from package bottom to photosensitive surface

KMPDA0626EB

Pin connections

Pin no.	Symbol	Function	I/O	Pin no.	Symbol	Function	I/O
A1	GND	Ground (CMOS)	I	C15	Out_Ep[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
A2	GND	Ground (CMOS)	I	C16	Out_Fp[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
A3	GND	Ground (CMOS)	I	C17	Out_Fp[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
A4	Vdd(D)	Digital supply voltage	I	C18	Out_Gp[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
A5	Vdd(D)	Digital supply voltage	I	C19	Out_Hp[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
A6	GND	Ground (CMOS)	I	C20	Out_Hp[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
A7	Vdd(C)	Counter supply voltage	I	C21	GND	Ground (CMOS)	I
A8	Vdd(C)	Counter supply voltage	I	D1	GND	Ground (CMOS)	I
A9	GND	Ground (CMOS)	I	D2	Vref3_a	Bias voltage for A/D converter	I
A10	GND	A/D converter ground	I	D3	GND	Ground (CMOS)	I
A11	GND	A/D converter ground	I	D4	CTRp_a	4-bit serializer sync signal	O
A12	GND	Ground (CMOS)	I	D5	Hsyncp_a	Line (horizontal) sync signal	O
A13	GND	Ground (CMOS)	I	D6	Out_An[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
A14	GND	Ground (CMOS)	I	D7	Out_An[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
A15	Vdd(D)	Digital supply voltage	I	D8	Out_Bn[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
A16	Vdd(D)	Digital supply voltage	I	D9	Out_Cn[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
A17	GND	Ground (CMOS)	I	D10	Out_Cn[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
A18	Vdd(D)	Digital supply voltage	I	D11	Out_Dn[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
A19	Vdd(D)	Digital supply voltage	I	D12	GND	Ground (CMOS)	I
A20	GND	Ground (CMOS)	I	D13	GND	Ground (CMOS)	I
A21	NC	-		D14	GND	Ground (CMOS)	I
B1	SPI_RSTB_a	SPI reset signal	I	D15	Out_En[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
B2	Vref1_a	Bias voltage for LVDS output	I	D16	Out_En[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
B3	GND	Ground (CMOS)	I	D17	Out_Fn[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
B4	Vsyncp_a	Frame (vertical) sync signal	O	D18	Out_Gn[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
B5	PCLKn_a	Pixel output sync signal	O	D19	Out_Gn[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
B6	Out_An[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	D20	Out_Hn[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
B7	Out_Bn[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	D21	Vref4_a	Bias voltage for A/D converter	O
B8	Out_Bn[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	E1	SPI_CS_a	SPI input signal (enable signal)	I
B9	Out_Cn[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	E2	Vref5_a	Bias voltage for A/D converter	O
B10	Out_Dn[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	E3	Vref6_a	Bias voltage for A/D converter	O
B11	Out_Dn[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	E4	CTRn_a	4-bit serializer sync signal	O
B12	GND	Ground (CMOS)	I	E5	Hsyncn_a	Line (horizontal) sync signal	O
B13	GND	Ground (CMOS)	I	E6	Out_Ap[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
B14	GND	Ground (CMOS)	I	E7	Out_Ap[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
B15	Out_En[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	E8	Out_Bp[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
B16	Out_Fn[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	E9	Out_Cp[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
B17	Out_Fn[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	E10	Out_Cp[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
B18	Out_Gn[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	E11	Out_Dp[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
B19	Out_Hn[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	E12	GND	Ground (CMOS)	I
B20	Out_Hn[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	E13	GND	Ground (CMOS)	I
B21	NC	-		E14	GND	Ground (CMOS)	I
C1	SPI_SCLK_a	SPI input signal (clock signal)	I	E15	Out_Ep[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
C2	Vref2_a	Bias voltage for LVDS output	O	E16	Out_Ep[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
C3	CLK	Master clock signal (30 MHz recommended)	I	E17	Out_Fp[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
C4	Vsyncn_a	Frame (vertical) sync signal	O	E18	Out_Gp[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
C5	PCLKp_a	Pixel output sync signal	O	E19	Out_Gp[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
C6	Out_Ap[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	E20	Out_Hp[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
C7	Out_Bp[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	E21	Vref7_a	Bias voltage for A/D converter	O
C8	Out_Bp[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	F1	SPI_MOSI_a	SPI input signal (setting input signal)	I
C9	Out_Cp[1]_a	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	F2	Vref8_a	Bias voltage for A/D converter	O
C10	Out_Dp[0]_a	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	F3	Vref9_a	Bias voltage for A/D converter	O
C11	Out_Dp[2]_a	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	F4	TG_reset	Timing circuit reset	I
C12	GND	Ground (CMOS)	I	F5	PLL_reset	Internal PLL reset signal	I
C13	GND	Ground (CMOS)	I	F17	GND	Ground (CMOS)	I
C14	GND	Ground (CMOS)	I	F18	GND	Ground (CMOS)	I

Pin no.	Symbol	Function	I/O	Pin no.	Symbol	Function	I/O
F19	GND	Ground (CMOS)	I	L4	SG_b	CCD summing gate_b	I
F20	NC	-		L5	P3V	CCD vertical register clock-3	I
F21	NC	-		L17	P2V	CCD vertical register clock-2	I
G1	GND	Ground (CMOS)	I	L18	SG_b	CCD summing gate_b	I
G2	GND	Ground (CMOS)	I	L19	A.GND	CCD ground voltage	I
G3	GND	Ground (CMOS)	I	L20	OFD	CCD overflow drain voltage	I
G4	GND	Ground (CMOS)	I	L21	A.GND	CCD ground voltage	I
G5	GND	Ground (CMOS)	I	M1	A.GND	CCD ground voltage	I
G17	GND	Ground (CMOS)	I	M2	RD	CCD reset drain voltage	I
G18	GND	Ground (CMOS)	I	M3	A.GND	CCD ground voltage	I
G19	GND	Ground (CMOS)	I	M4	RG_b	CCD reset gate_b	I
G20	GND	Ground (CMOS)	I	M5	P4V	CCD vertical register clock-4	I
G21	GND	Ground (CMOS)	I	M17	P1V	CCD vertical register clock-1	I
H1	A.GND	CCD ground voltage	I	M18	RG_b	CCD reset gate_b	I
H2	OD	CCD output drain voltage	I	M19	A.GND	CCD ground voltage	I
H3	A.GND	CCD ground voltage	I	M20	OD	CCD output drain voltage	I
H4	A.GND	CCD ground voltage	I	M21	A.GND	CCD ground voltage	I
H5	A.GND	CCD ground voltage	I	N1	A.GND	CCD ground voltage	I
H17	A.GND	CCD ground voltage	I	N2	RD	CCD reset drain voltage	I
H18	A.GND	CCD ground voltage	I	N3	A.GND	CCD ground voltage	I
H19	A.GND	CCD ground voltage	I	N4	A.GND	CCD ground voltage	I
H20	RD	CCD reset drain voltage	I	N5	A.GND	CCD ground voltage	I
H21	A.GND	CCD ground voltage	I	N17	A.GND	CCD ground voltage	I
I1	A.GND	CCD ground voltage	I	N18	A.GND	CCD ground voltage	I
I2	OD	CCD output drain voltage	I	N19	A.GND	CCD ground voltage	I
I3	A.GND	CCD ground voltage	I	N20	OD	CCD output drain voltage	I
I4	RG_a	CCD reset gate_a	I	N21	A.GND	CCD ground voltage	I
I5	P1V	CCD vertical register clock-1	I	O1	GND	Ground (CMOS)	I
I17	P4V	CCD vertical register clock-4	I	O2	GND	Ground (CMOS)	I
I18	RG_a	CCD reset gate_a	I	O3	GND	Ground (CMOS)	I
I19	A.GND	CCD ground voltage	I	O4	GND	Ground (CMOS)	I
I20	RD	CCD reset drain voltage	I	O5	GND	Ground (CMOS)	I
I21	A.GND	CCD ground voltage	I	O17	GND	Ground (CMOS)	I
J1	A.GND	CCD ground voltage	I	O18	GND	Ground (CMOS)	I
J2	OFD	CCD overflow drain voltage	I	O19	GND	Ground (CMOS)	I
J3	A.GND	CCD ground voltage	I	O20	GND	Ground (CMOS)	I
J4	SG_a	CCD summing gate_a	I	O21	GND	Ground (CMOS)	I
J5	P2V	CCD vertical register clock-2	I	P1	NC	-	
J17	P3V	CCD vertical register clock-3	I	P2	NC	-	
J18	SG_a	CCD summing gate_a	I	P3	GND	Ground (CMOS)	I
J19	A.GND	CCD ground voltage	I	P4	GND	Ground (CMOS)	I
J20	OFG	CCD overflow gate voltage	I	P5	GND	Ground (CMOS)	I
J21	A.GND	CCD ground voltage	I	P17	PLL_reset	Internal PLL reset signal	I
K1	A.GND	CCD ground voltage	I	P18	TG_reset	Timing circuit reset	I
K2	OG	CCD output gate voltage	I	P19	Vref9_b	Bias voltage for A/D converter	O
K3	OS(test)_4*34	CCD output transistor source (test)_4	O	P20	Vref8_b	Bias voltage for A/D converter	O
K4	OS(test)_3*34	CCD output transistor source (test)_3	O	P21	SPI_MOSI_b	SPI input signal (setting input signal)	I
K5	A.GND	CCD ground voltage	I	Q1	Vref7_b	Bias voltage for A/D converter	O
K17	A.GND	CCD ground voltage	I	Q2	Out_Hp[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
K18	OS(test)_1*34	CCD output transistor source (test)_1	O	Q3	Out_Gp[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
K19	OS(test)_2*34	CCD output transistor source (test)_2	O	Q4	Out_Gp[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
K20	OG	CCD output gate voltage	I	Q5	Out_Fp[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
K21	A.GND	CCD ground voltage	I	Q6	Out_Ep[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
L1	A.GND	CCD ground voltage	I	Q7	Out_Ep[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
L2	OFG	CCD overflow gate voltage	I	Q8	GND	Ground (CMOS)	I
L3	A.GND	CCD ground voltage	I	Q9	GND	Ground (CMOS)	I

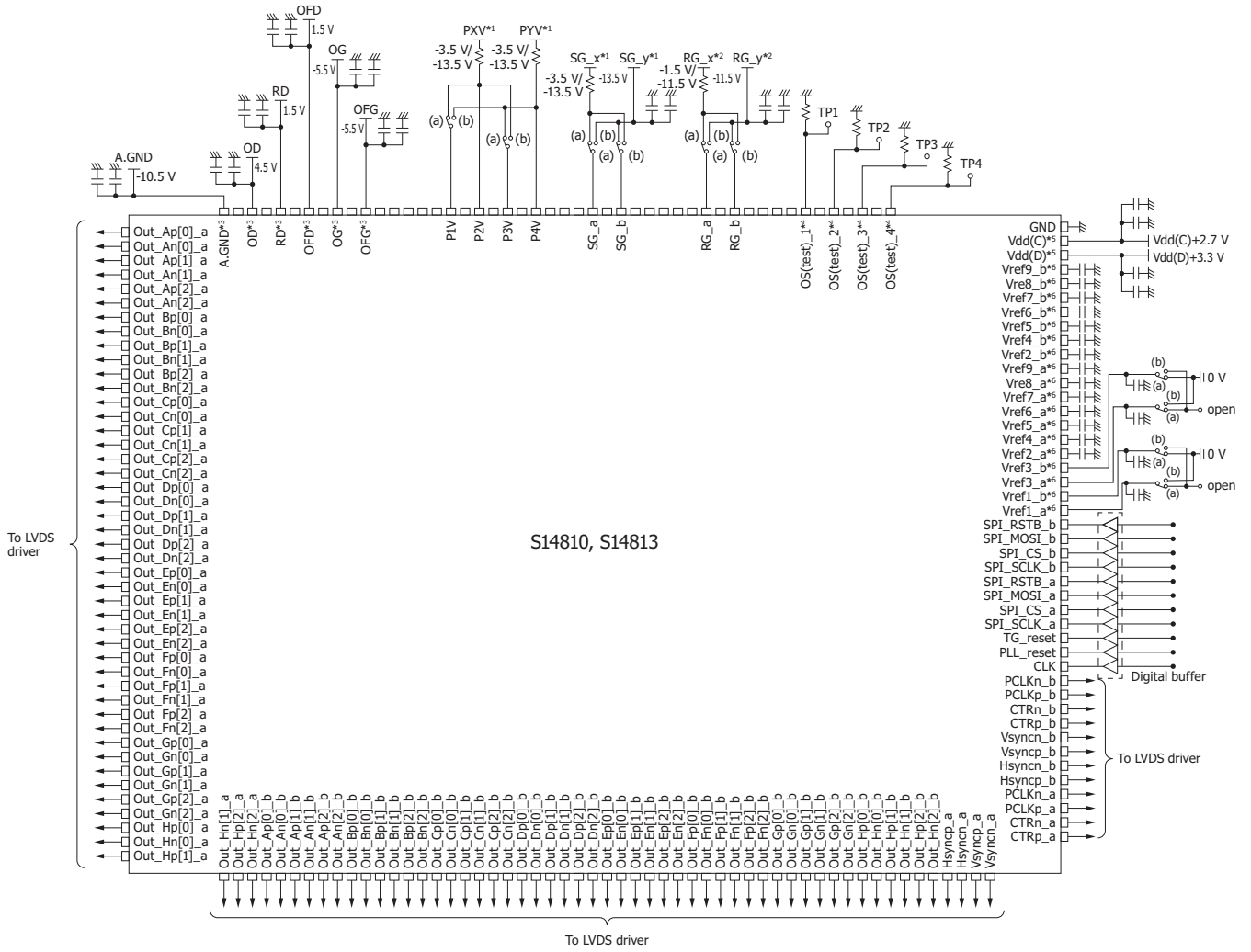
*34: Leave OS terminals open.

Pin no.	Symbol	Function	I/O	Pin no.	Symbol	Function	I/O
Q10	GND	Ground (CMOS)	I	S16	Out_Ap[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
Q11	Out_Dp[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	S17	PCLKp_b	Pixel output sync signal	O
Q12	Out_Cp[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	S18	Vsyncn_b	Frame (vertical) sync signal	O
Q13	Out_Cp[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	S19	CLK	Master clock signal (30 MHz recommended)	I
Q14	Out_Bp[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	S20	Vref2_b	Bias voltage for LVDS output	O
Q15	Out_Ap[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	S21	SPI_SCLK_b	SPI input signal (clock signal)	I
Q16	Out_Ap[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	T1	NC	-	
Q17	Hsyncn_b	Line (horizontal) sync signal	O	T2	Out_Hn[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
Q18	CTRn_b	4-bit serializer sync signal	O	T3	Out_Hn[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
Q19	Vref6_b	Bias voltage for A/D converter	O	T4	Out_Gn[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
Q20	Vref5_b	Bias voltage for A/D converter	O	T5	Out_Fn[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
Q21	SPI_CS_b	SPI input signal (enable signal)	I	T6	Out_Fn[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
R1	Vref4_b	Bias voltage for A/D converter	O	T7	Out_En[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
R2	Out_Hn[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	T8	GND	Ground (CMOS)	I
R3	Out_Gn[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	T9	GND	Ground (CMOS)	I
R4	Out_Gn[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	T10	GND	Ground (CMOS)	I
R5	Out_Fn[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	T11	Out_Dn[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
R6	Out_En[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	T12	Out_Dn[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
R7	Out_En[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	T13	Out_Cn[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
R8	GND	Ground (CMOS)	I	T14	Out_Bn[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
R9	GND	Ground (CMOS)	I	T15	Out_Bn[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
R10	GND	Ground (CMOS)	I	T16	Out_An[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
R11	Out_Dn[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	T17	PCLKn_b	Pixel output sync signal	O
R12	Out_Cn[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	T18	Vsyncp_b	Frame (vertical) sync signal	O
R13	Out_Cn[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	T19	GND	Ground (CMOS)	I
R14	Out_Bn[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	T20	Vref1_b	Bias voltage for LVDS output	I
R15	Out_An[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	T21	SPI_RSTB_b	SPI reset signal	I
R16	Out_An[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	U1	NC	-	
R17	Hsyncp_b	Line (horizontal) sync signal	O	U2	GND	Ground (CMOS)	I
R18	CTRp_b	4-bit serializer sync signal	O	U3	Vdd(D)	Digital supply voltage	I
R19	GND	Ground (CMOS)	I	U4	Vdd(D)	Digital supply voltage	I
R20	Vref3_b	Bias voltage for A/D converter	I	U5	GND	Ground (CMOS)	I
R21	GND	Ground (CMOS)	I	U6	Vdd(D)	Digital supply voltage	I
S1	GND	Ground (CMOS)	I	U7	Vdd(D)	Digital supply voltage	I
S2	Out_Hp[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	U8	GND	Ground (CMOS)	I
S3	Out_Hp[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	U9	GND	Ground (CMOS)	I
S4	Out_Gp[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	U10	GND	Ground (CMOS)	I
S5	Out_Fp[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	U11	GND	A/D converter ground	I
S6	Out_Fp[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	U12	GND	A/D converter ground	I
S7	Out_Ep[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	U13	GND	Ground (CMOS)	I
S8	GND	Ground (CMOS)	I	U14	Vdd(C)	Counter supply voltage	I
S9	GND	Ground (CMOS)	I	U15	Vdd(C)	Counter supply voltage	I
S10	GND	Ground (CMOS)	I	U16	GND	Ground (CMOS)	I
S11	Out_Dp[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	U17	Vdd(D)	Digital supply voltage	I
S12	Out_Dp[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	U18	Vdd(D)	Digital supply voltage	I
S13	Out_Cp[1]_b	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O	U19	GND	Ground (CMOS)	I
S14	Out_Bp[2]_b	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O	U20	GND	Ground (CMOS)	I
S15	Out_Bp[0]_b	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O	U21	GND	Ground (CMOS)	I

Note: The video output symbol is defined as follows.

Out_An[0]
- [0]: 0, 1, 2, 3-bits, [1]: 4, 5, 6, 7-bits, [2]: 8, 9, 10, 11-bits
- p: positive input of differential pair, n: negative input of differential pair
- A to H: output ports

Application circuit example



*1: 10 Ω
*2: 100 Ω
*3: Connect 0.1 μF and 10 μF.
*4: Connect 100 kΩ.
*5: Connect 0.1 μF and 10 μF.
*6: Connect 0.1 μF.

Note: Set switch to (a) side during A port readout. Set switch to (b) side during B port readout.

KMPDC0811EB

Precautions (electrostatic countermeasures)

· Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
· Do not place the sensor directly on workbenches or the like that may become charged with static electricity.
· Connect a ground wire to workbenches or floors in order to discharge static electricity.
· Ground tools, such as tweezers and soldering irons, that are used to handle the sensor.

It is not always necessary to provide all the anti-electrostatic measures stated above. Implement these countermeasures according to the extent of deterioration or damage that may occur.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

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Cat. No. KMPD1216E03 Jul. 2021 DN