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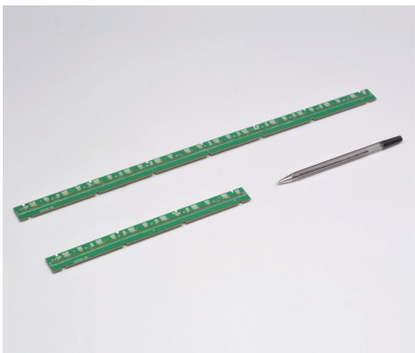
NEW

CMOS linear image sensors



S11720 series

Long photosensitive area image sensors with CMOS chips arranged in a single row

The S11720 series is a CMOS linear image sensor developed for close contact optical systems. This long photosensitive area image sensor with CMOS chips arranged in a row allows a wide range of readout with one camera unit [195 mm (S11720-20), 390 mm (S11720-40)]. It also enables high sensitivity (40800 V/*lx*·s) and high-speed readout (45.4 klines/s).

Features

- **Pixel size: 127 × 127 µm**
- **Number of pixels:**
  1536 (256 × 6 chips): S11720-20
  3072 (256 × 12 chips): S11720-40
- **Effective photosensitive area length:**
  194.97 mm: S11720-20
  390.04 mm: S11720-40
- **High-speed readout: 45.4 klines/s**
- **High sensitivity: 40800 V/*lx*·s (gain=8)**
- **Simultaneous integration of all pixels**
- **5 V power supply operation**
- **SPI communication function**
- **Built-in 16-bit A/D converter**

Applications

- **Film inspection**
- **Printed circuit board appearance inspection**
- **Print inspection**
- **Industrial line camera**

Structure

Parameter	S11720-20	S11720-40	Unit
Number of pixels	1536 (256 × 6)	3072 (256 × 12)	-
Pixel pitch	127		µm
Pixel height	127		µm
Effective photosensitive area length	194.972	390.044	mm
Package	Glass epoxy		-
Seal material	Silicone resin		-

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Condition	Value	Unit
Supply voltage	Vdd		-0.3 to +6	V
CMOS clock pulse voltage	V(CCLK)		-0.3 to +6	V
CMOS start pulse voltage	V(CST)		-0.3 to +6	V
CMOS gain selection voltage	V(CVG1)		-0.3 to +6	V
	V(CVG2)			
SPI pulse voltage	V(SCLK)		-0.3 to +3.55	V
	V(SEN1)			
	V(SEN2)			
	V(SEN3)			
	V(SEN4)			
	V(SDIO)			
Reset pulse voltage	V(RES)		-0.3 to +3.55	V
Operating temperature	Topr	No dew condensation*1	0 to +70	°C
Storage temperature	Tstg	No dew condensation*1	-20 to +70	°C

*1: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.75	5	5.25	V
CMOS clock pulse voltage	High level	V(CCLK)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	
CMOS start pulse voltage	High level	V(CST)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	
CMOS gain selection voltage	High level	V(CVG1) V(CVG2)	3	Vdd	Vdd + 0.25	V
	Low level		0	-	0.3	
SPI pulse voltage	High level	V(SCLK) V(SEN1) V(SEN2) V(SEN3) V(SEN4) V(SDIO)	2	3.3	3.5	V
	Low level		0	-	0.8	
Reset pulse voltage	High level	V(RES)	2	3.3	3.5	V
	Low level		0	-	0.8	

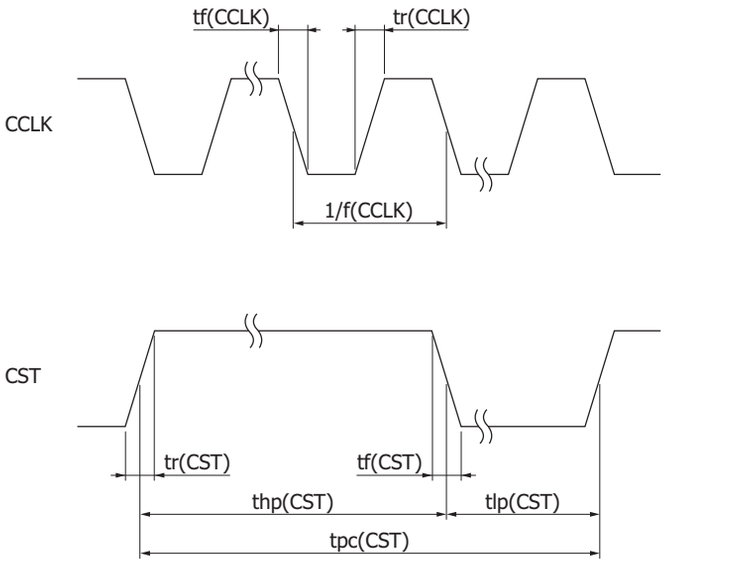
Electrical characteristics

Digital input signal

(Ta=25 °C, Vdd=5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CMOS clock pulse frequency	f(CCLK)	10	13	15	MHz
CMOS clock pulse duty period	D(CCLK)	45	50	55	%
CMOS start pulse period	tpi(CST)	102/f(CCLK)	-	-	s
CMOS high start pulse period	thp(CST)	6/f(CCLK)	-	-	s
CMOS low start pulse period	tlp(CST)	96/f(CCLK)	-	-	s
CMOS clock pulse rise/fall times	tr(CCLK) tf(CCLK)	-	5	7	ns
CMOS start pulse rise/fall times	tr(CST) tf(CST)	-	5	7	ns

■ CCLK/CST input timing

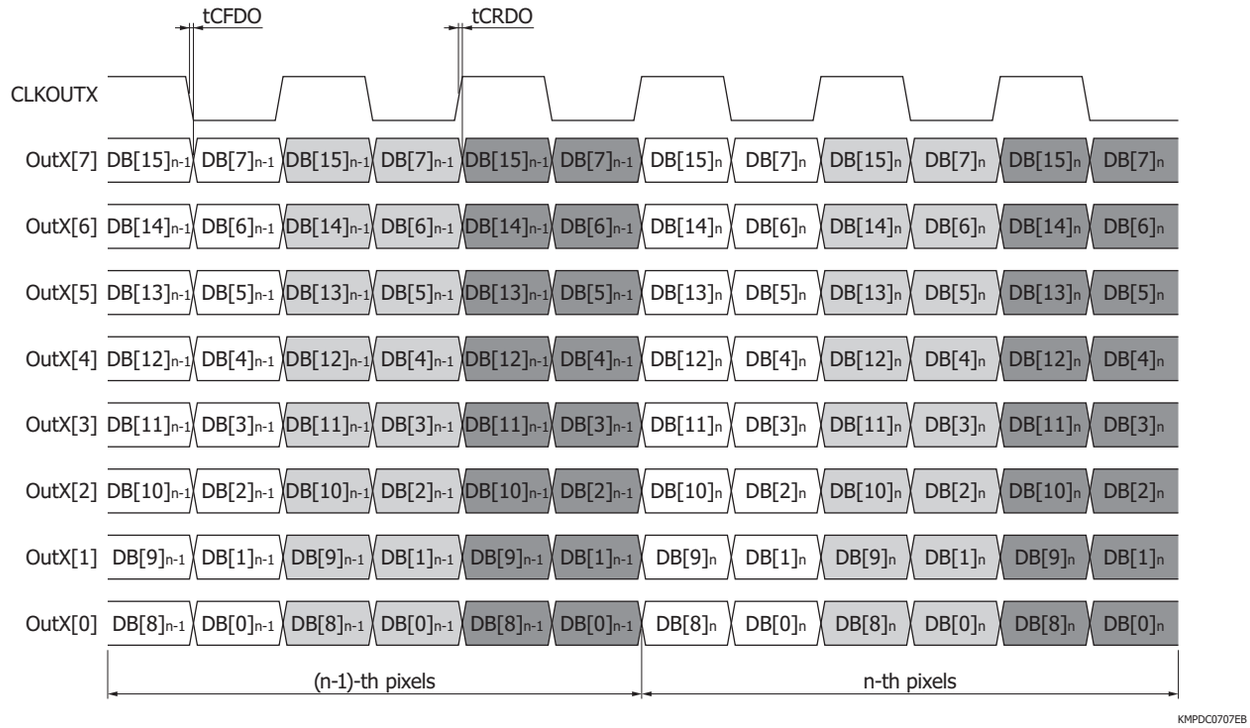


Digital output signal

[Ta=25 °C, Vdd=5 V, f (CCLK)=15 MHz]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Data rate		DR		f(CCLK) × 6		Hz
Line rate		LR	-	-	45.4	klines/s
CMOS output voltage	High level	V(OutX) V(CLKOUTX)	2.95	-	-	V
	Low level		-	-	0.25	
tCFDO		-	-2.83	-	2.7	ns
tCRDO		-	-2.83	-	2.7	ns

■ Synchronous signal, video signal



· OutX[Y] (Y=0 to 7): video output
DB [Z] (Z= 0 to 15-bit): 16-bit video output

Current consumption

[Ta=25 °C, Vdd=5 V, f(CCLK)=15 MHz, dark state]

Parameter	Symbol	S11720-20			S11720-40			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption	Ic	-	530	630	-	1060	1260	mA

Electrical characteristics of A/D converter [Ta=25 °C, Vdd=5 V, f(CCLK)=15 MHz]

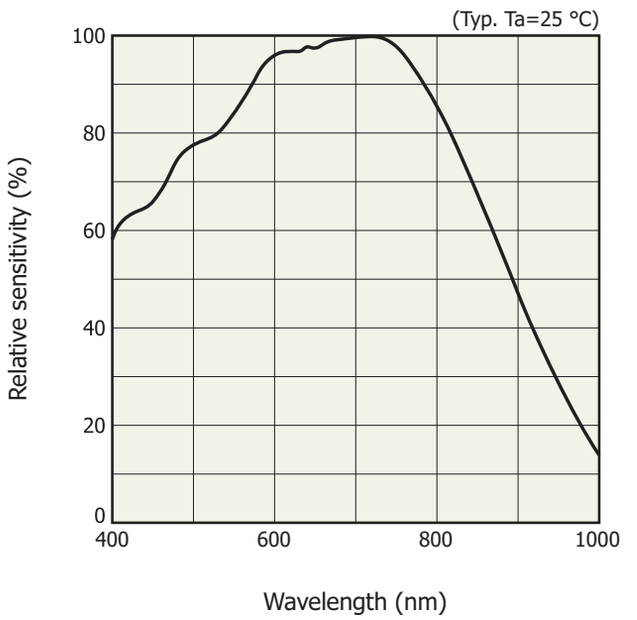
Parameter	Symbol	Specification	Unit
Resolution	RESO	16	bit
Conversion voltage range	-	2.4 (0.26 to 2.66)	V

Electrical and optical characteristics [Ta=25 °C, Vdd=5 V, f(CCLK)=15 MHz, LR=45.4 klines/s]

Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Spectral response range	λ	-		400 to 1000		nm
Peak sensitivity wavelength	λp	-	-	700	-	nm
Photosensitivity*2	Sw	1	-	5100	-	V/(*lx*·s)
			-	139M	-	DN/(*lx*·s)
		8	-	40800	-	V/(*lx*·s)
			-	1114M	-	DN/(*lx*·s)
Conversion efficiency	CE	1	-	25	-	μV/e^-
			-	0.7	-	DN/e^-
		8	-	200	-	μV/e^-
			-	5.7	-	DN/e^-
Dark output*3 *4	VD	1	0	0.25	1.25	mV
			0	6.84	34.13	DN
		8	0	2	10	mV
			0	54.7	27.3	DN
Saturation output	Vsat	1	1.2	1.4	2.2	V
			32768	38229	60074	DN
		8	1.8	2.0	2.4	V
			49152	54613	65535	DN
Readout noise*5	Nread	1	-	0.6	3	mV rms
			-	16	82	DN rms
		8	-	1.5	8	mV rms
			-	41	218	DN rms
Dynamic range*6	Drange	1	-	2333	-	-
		8	-	1333	-	
Output offset voltage	Voffset	-	-	0.3	-	V
			-	8192	-	DN
Photoresponse nonuniformity*7	PRNU	1	-	±10	±20	%
		8	-	±10	±20	
Image lag*8	Lag	-	-	-	2	%

*2: 2856 K, tungsten lamp
*3: Ts=10 μs
*4: Voltage difference from the Voffset
*5: Dark state
*6: Vsat/Nread
*7: The output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. It is defined as follows for the 1530 pixels (S11720-20) and 3066 pixels (S11720-40) excluding the 3 pixels at each end of the sensor.
PRNU = (ΔX/X) × 100 [%]
*8: Signal components of the preceding line data that still remain even after the data is read out in a saturation output state. Image lag increases when the output exceeds the saturation output voltage.
Note: DN (digital number): unit of A/D converter output.

Spectral response (typical example)



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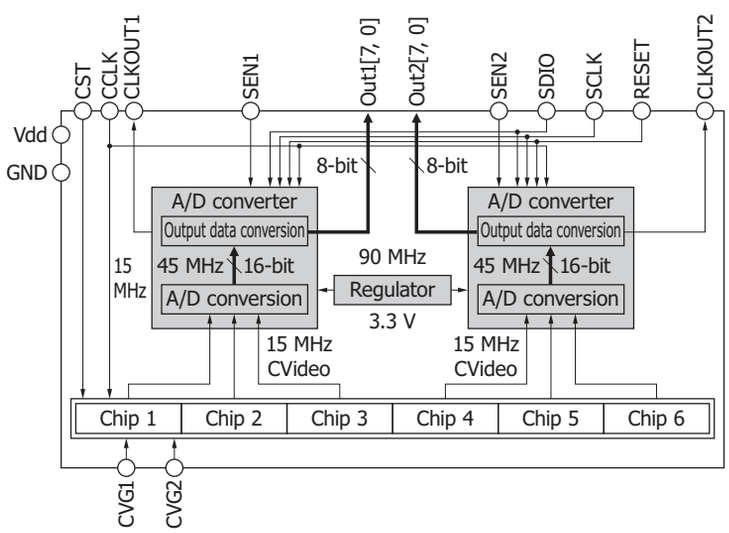
Block diagram

S11720-20



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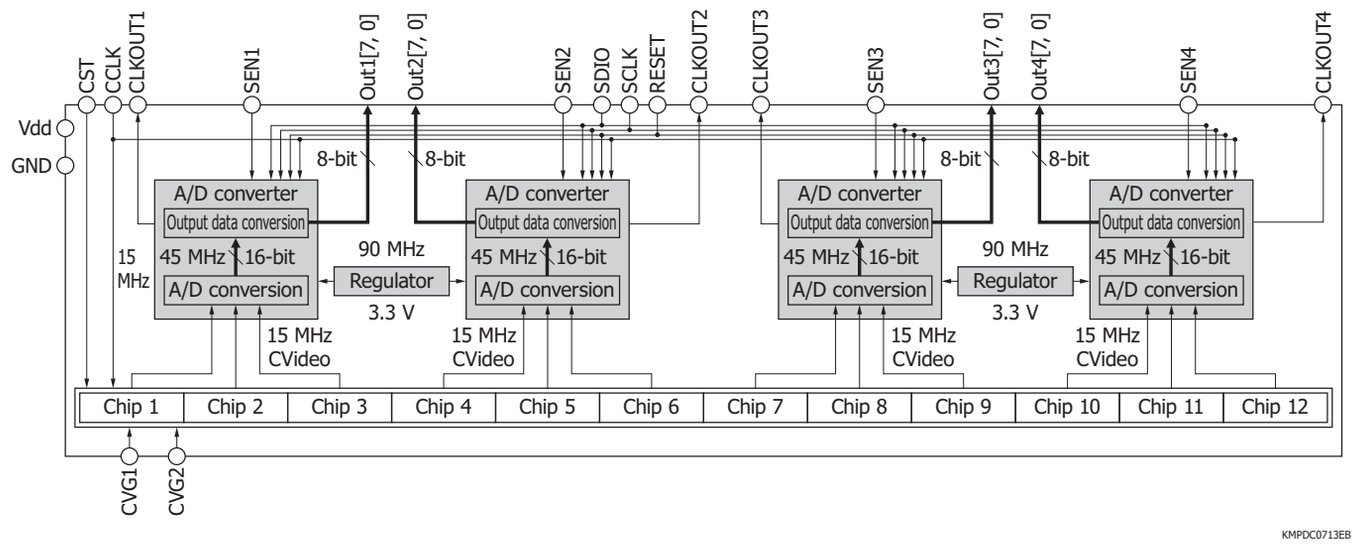
S11720-40



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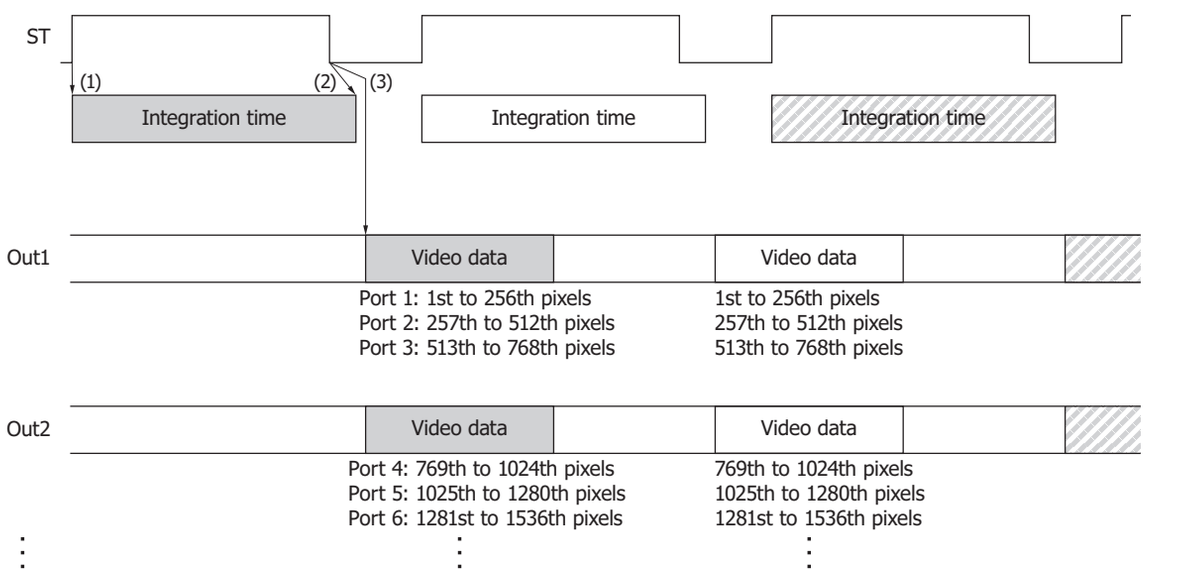
Timing chart

■ Description of operation

The integration time is determined by the high period of the start pulse.



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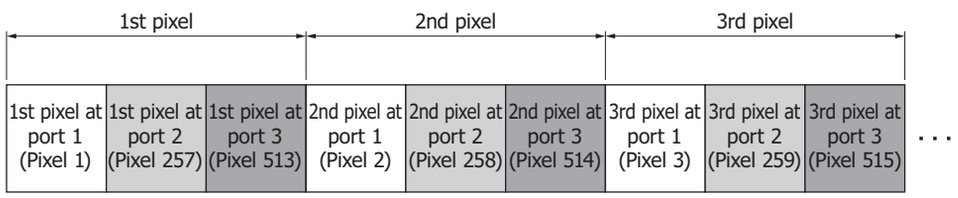
(1) The start of integration time is determined by the rising edge of the start pulse.
(2) The end of integration time is determined by the falling edge of the start pulse.
(3) Video data is output after the falling edge of the start pulse.
Video data is output in order from the first pixel of each port in the following order.
Ex.: 1st pixel (port 1 → port 2 → port 3), 2nd pixel (port 1 → port 2 → port 3), 3rd pixel (port 1…



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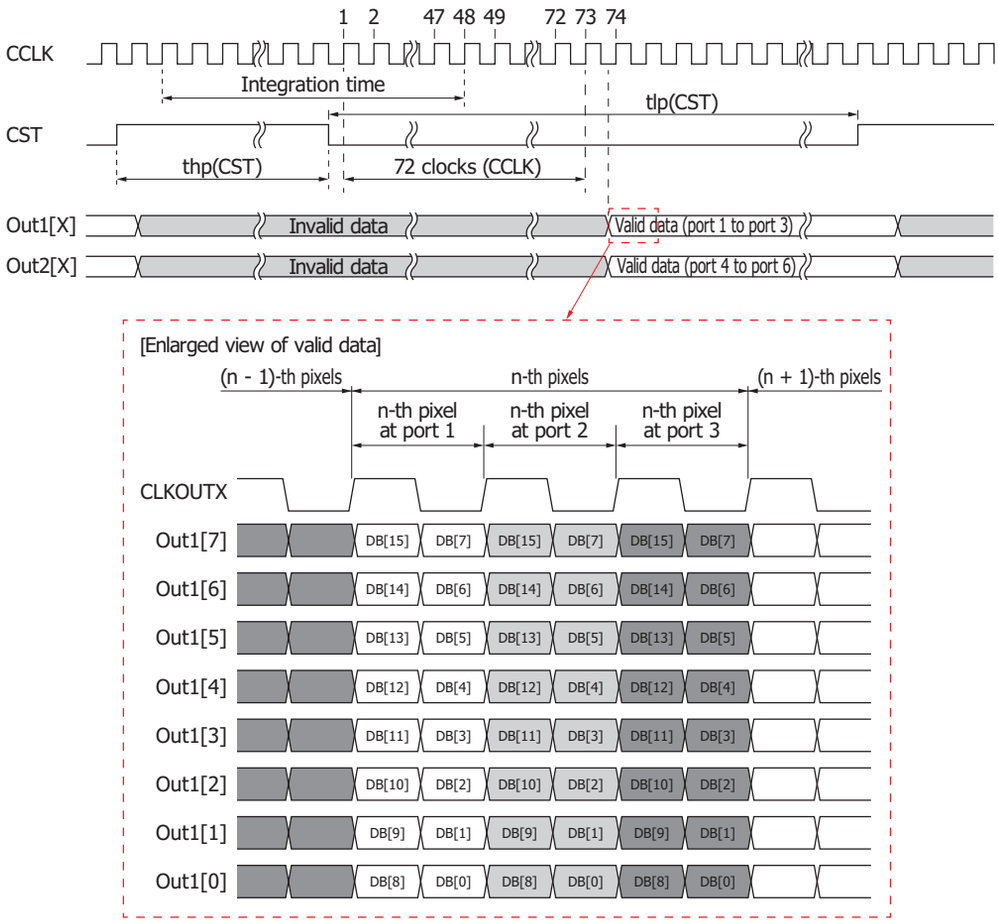
Note: Signal integration is possible even during video output.

S11720-20



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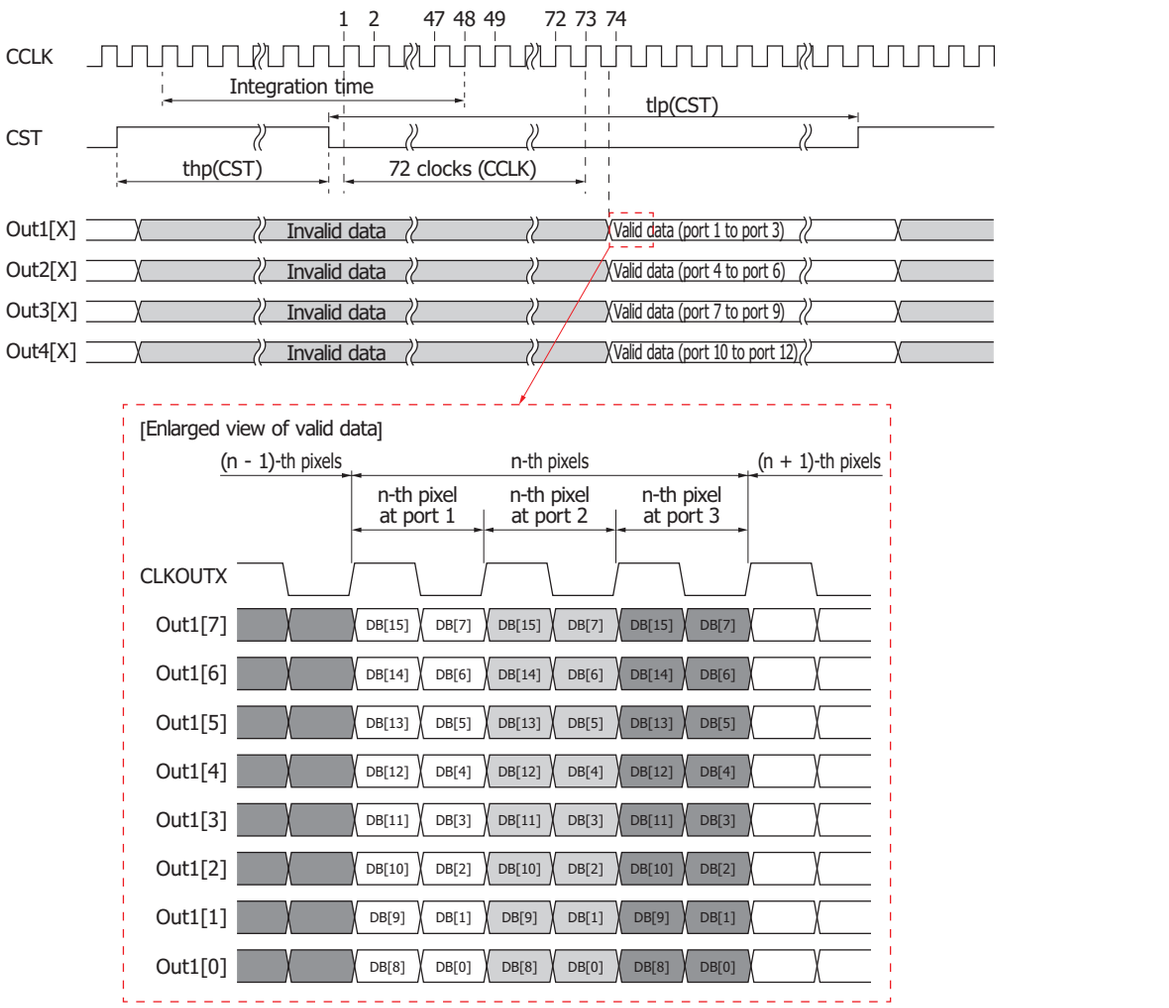
S11720-40



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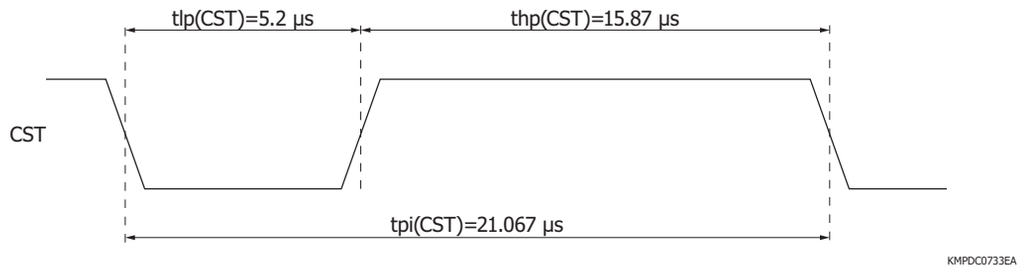
· The integration time equals to high period of CST start pulse plus 45 clock cycles of CCLK.
· Effective data for Out1[X] is repeatedly output in order of port 1 (n-th pixel) → port 2 (n-th pixel) → port 3 (n-th pixel) → port 1 [(n + 1)-th pixel].
· Out1[X] (X=1 to 7): video output (Likewise Out2[X], Out3[X], Out4)
DB[Z] (Z=0 to 15-bit): 16-bit video output

Operating example

When CMOS clock pulse frequency is maximized, the time of one scan is minimized (line rate: 45.45 klines/s max.), and the integration time is maximized.



· CMOS clock pulse frequency=15 MHz
· CMOS start pulse interval=330/f(CCLK)=330/15 MHz=22.0 µs
· CMOS start pulse high period =start pulse interval - minimum start pulse low period
=330/f(CCLK) - 96/f(CCLK)=330/15 MHz - 96/15 MHz=15.6 µs
· The integration time=start pulse high period + 45 cycles of clock pulse
=15.6 + 3.0=18.6 µs

Gain setting

Set sensor gain with CVG1, and CVG2.

V(CVG1)	V(CVG2)	Gain
Low level	Low level	8
Low level	High level	5
High level	Low level	2
High level	High level	1

SPI default settings

The SPI default settings procedures for the S11720-20 are shown as follows. (For the S11720-40, set defaults for SEN1, SEN2, SEN3, and SEN4.)
Supply 5 V to Vdd and input CCLK. After setting Reset to low for a period of 3CLK or more in CCLK, lock the Reset on high. This will be the default settings for the A/D converter register.
Next, input to SPI (binary) using SCLK, SEN1, SEN2 and SDIO following the setting order in the table below.
Then, lock SEN1 and SEN2 on high and input the rising edge signal to SDIO twice to begin operation.
When not setting the SPI input, set the SDIO to High for a period equal to only 4 CCLK clocks immediately after the CST pulse rises, and set all other periods to Low.

Setting order	Parameter	Address		Input value	
		Binary	Decimal	Binary	Decimal
1	Page Register	11111	31	0000 0000	0
2	Main Configuration0	00000	0	1111 0001	241
3	Main Configuration1	00001	1	0010 1110	46
4	Main Configuration2	00010	2	0010 1000	40
5	Page Register	11111	31	0000 0010	2
6	SH Pulse Width	00001	1	0000 0100	10
7	CMOS Data Mode Status Bit	11110	30	0010 0000	32
8	Page Register	11111	31	0000 0011	3
9	Output Mapping CLK10	00100	4	0000 1111	15
10	Page Register	11111	31	0000 0000	0
11	OSR SAMPLE Control	01111	15	0001 0011	20
12	OSG SAMPLE Control	10000	16	0001 0011	20
13	OSB SAMPLE Control	10001	17	0001 0011	20
14	VCLP Configuration	00111	7	0001 0000	16
15	Main Configuration2	00010	2	0000 1001	9

Note: Always set to the address in the above table. Setting using an address not in the table above may cause malfunctions.

Setting the SPI A/D converter gain and offset

S11720-20

After the default setting for the A/D converter, the Page Register will switch to "1." Input address 11111 and value 0000 0001 in SEN1 and SEN2. Then, input the required address and the following two values.
ADC gain: Gain[V/V]=196/(280 - "PGA input value")
ADC offset: offset[DN]=("offset input value"- 64) × 16

ADC	Register	Address (Binary)	Default value (Binary)
SEN1	PGA (port 1) [7:0]	00000	0101 0100
SEN1	PGA (port 2) [7:0]	00001	0101 0100
SEN1	PGA (port 3) [7:0]	00010	0101 0100
SEN2	PGA (port 4) [7:0]	00000	0101 0100
SEN2	PGA (port 5) [7:0]	00001	0101 0100
SEN2	PGA (port 6) [7:0]	00010	0101 0100
SEN1	Offset (port 1) [6:0]	01111	0100 0000
SEN1	Offset (port 2) [6:0]	10000	0100 0000
SEN1	Offset (port 3) [6:0]	10001	0100 0000
SEN2	Offset (port 4) [6:0]	01111	0100 0000
SEN2	Offset (port 5) [6:0]	10000	0100 0000
SEN2	Offset (port 6) [6:0]	10001	0100 0000

Note: Always set to the address in the above table. Setting using an address not in the table above may cause malfunctions.

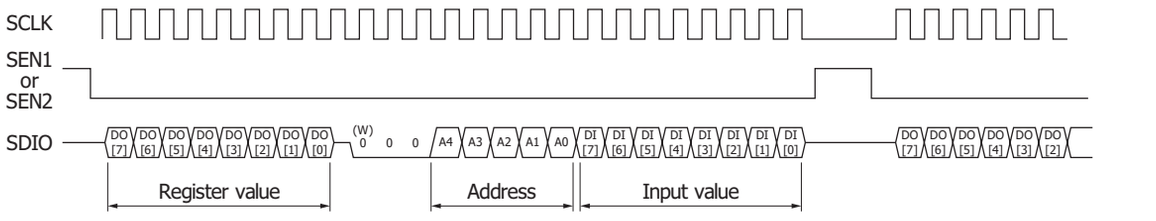
S11720-40

After the default setting for the A/D converter, the Page Register will switch to "1." Input address 11111 and value 0000 0001 in SEN1, SEN2, SEN3, and SEN4. Then, input the required address and the following two values.
Gain in ADC: Gain[V/V]=196/(280 - "PGA input value")
Offset in ADC: offset[DN]=("offset input value" - 64) × 16

ADC	Register	Address (Binary)	Default value (Binary)
SEN1	PGA (port 1) [7:0]	00000	0101 0100
SEN1	PGA (port 2) [7:0]	00001	0101 0100
SEN1	PGA (port 3) [7:0]	00010	0101 0100
SEN2	PGA (port 4) [7:0]	00000	0101 0100
SEN2	PGA (port 5) [7:0]	00001	0101 0100
SEN2	PGA (port 6) [7:0]	00010	0101 0100
SEN3	PGA (port 7) [7:0]	00000	0101 0100
SEN3	PGA (port 8) [7:0]	00001	0101 0100
SEN3	PGA (port 9) [7:0]	00010	0101 0100
SEN4	PGA (port 10) [7:0]	00000	0101 0100
SEN4	PGA (port 11) [7:0]	00001	0101 0100
SEN4	PGA (port 12) [7:0]	00010	0101 0100
SEN1	Offset (port 1) [6:0]	01111	0100 0000
SEN1	Offset (port 2) [6:0]	10000	0100 0000
SEN1	Offset (port 3) [6:0]	10001	0100 0000
SEN2	Offset (port 4) [6:0]	01111	0100 0000
SEN2	Offset (port 5) [6:0]	10000	0100 0000
SEN2	Offset (port 6) [6:0]	10001	0100 0000
SEN3	Offset (port 7) [6:0]	01111	0100 0000
SEN3	Offset (port 8) [6:0]	10000	0100 0000
SEN3	Offset (port 9) [6:0]	10001	0100 0000
SEN4	Offset (port 10) [6:0]	01111	0100 0000
SEN4	Offset (port 11) [6:0]	10000	0100 0000
SEN4	Offset (port 12) [6:0]	10001	0100 0000

Note: Always set to the address in the above table. Setting using an address not in the table above may cause malfunctions.

SPI input timing (write)



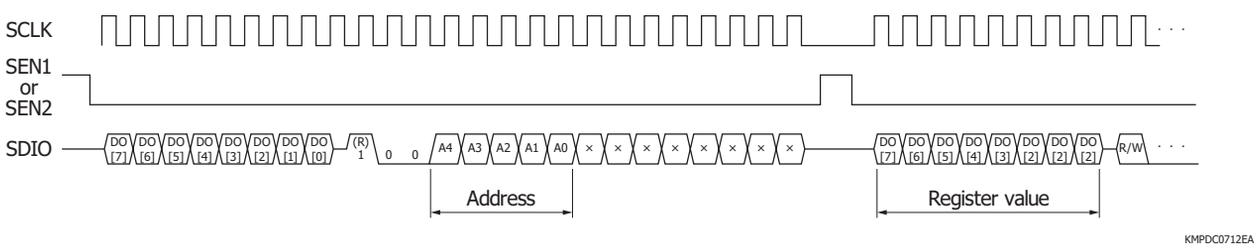
· Use the following to set the SPI.
  S11720-20: SCLK, SEN1, SEN2, SDIO, Reset,
  S11720-40: SCLK, SEN1, SEN2, SEN3, SEN4, SDIO, Reset
· Select the A/D converter in SEN1/SEN2 and change the settings.
· SEN1 is for ADC1 (ports 1 to 3), and SEN2 is for ADC2 (ports 4 to 6).
· SDIO settings are effective when SEN1/SEN2 are in their low period.
· Input an address and values into SDIO that match the Main Configuration, PGA, Offset, etc.
· Setting Reset to low level resets all parameters.
· The register value is the value at previously addressed register regardless of the write/readout.

(Ta=25 °C, Vdd=5 V, f(CCLK)=15 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock pulse frequency	f(SCLK)	10	13	15	MHz
SPI clock pulse duty cycle	D(SCLK)	-	50	-	%
SPI setup time (SEN1, SEN2, SEN3, SEN4)	tSET(SEN)	1.25	-	-	ns
SPI hold time (SEN1, SEN2, SEN3, SEN4)	tHOLD(SEN)	2.82	-	-	ns
SPI setup time (SDIO)	tSET(SDIO)	4	-	-	ns
SPI hold time (SDIO)	tHOLD(SDIO)	1	-	-	ns
SEN pulse high period (SEN1, SEN2, SEN3, SEN4)	thp(SEN)	4/f(CCLK)	-	-	s
Digital input signal rise time*9	tr(sigi)	-	10	30	ns
Digital input signal fall time*9	tf(sigi)	-	10	30	ns

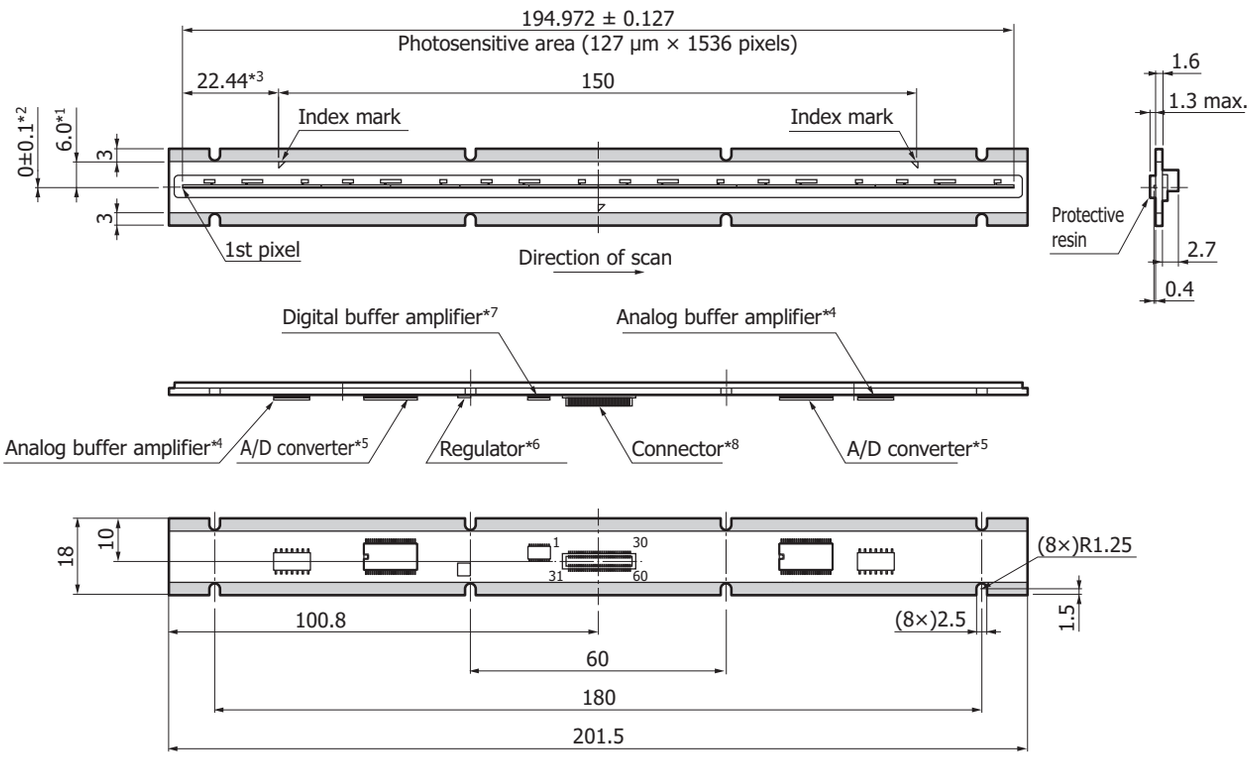
*9: Time for the input voltage to rise or fall between 10% and 90%

SPI input timing (readout)



Dimensional outline (unit: mm)

S11720-20



Tolerance unless otherwise noted: ±0.2

Parts unmounted area

*1: Distance from the fiducial point to photosensitive area center

*2: Variation for Y direction at pixel center

*3: Distance from the fiducial point to the first pixel center

*4: ADA4891-3ARZ (Analog Device)

*5: LM98714CCMT/NOPB (Texas Instruments)

*6: ADM7171ACPZ-3.3-R7 (Analog Devices)

*7: TC74VHC541FK (Toshiba Electronic Devices & Storage Corporation)

*8: DF12B-60DS-0.5 V (86) [HIROSE ELECTRIC]

Note: Fiducial point: Refer to "Enlarged view of index mark" (P.14).

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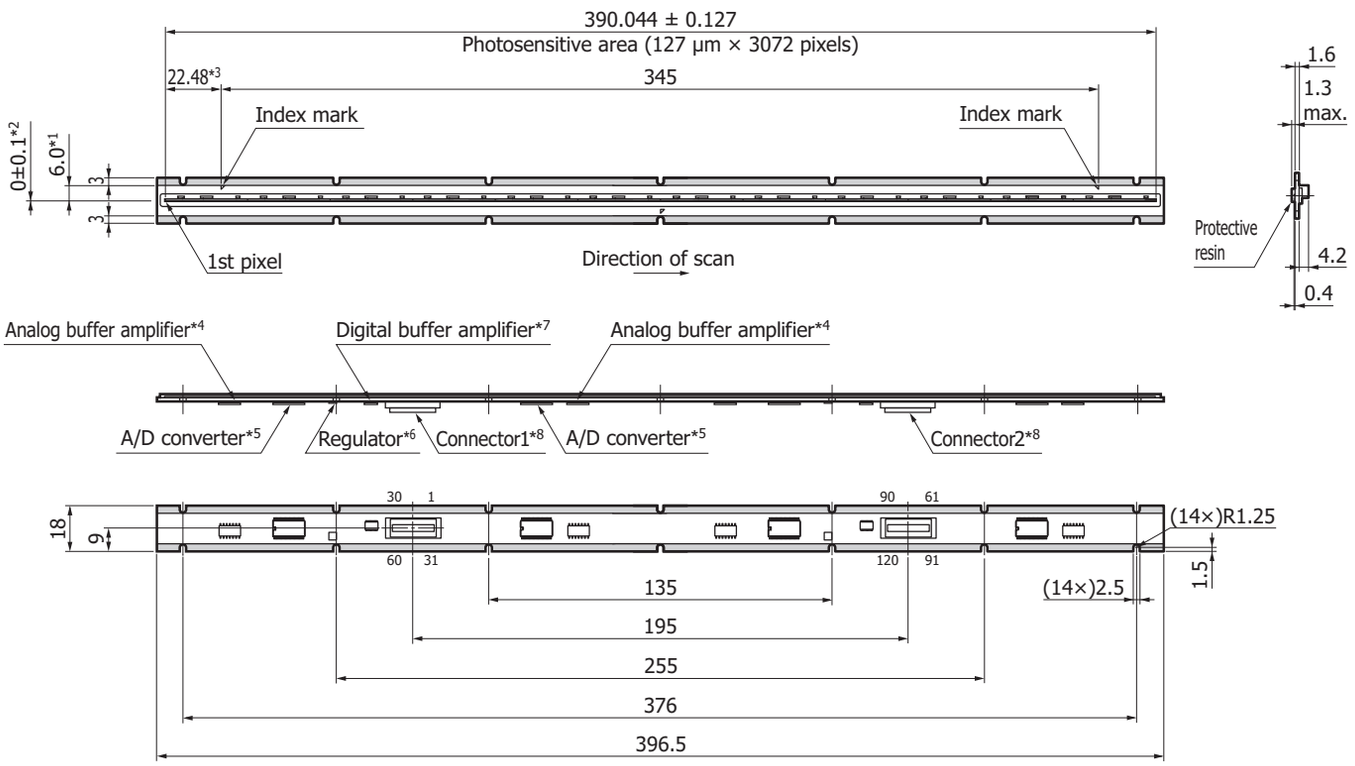
S11720-40



Tolerance unless otherwise noted: ±0.2
Parts unmounted area
*1: Distance from the fiducial point to photosensitive area center
*2: Variation for Y direction at pixel center
*3: Distance from the fiducial point to the first pixel center
*4: ADA4891-3ARZ (Analog Device)
*5: LM98714CCMT/NOPB (Texas Instruments)
*6: ADM7171ACPZ-3.3-R7 (Analog Devices)
*7: TC74VHC541FK (Toshiba Electronic Devices & Storage Corporation)
*8: DY00-060S (KEL)
Note: Fiducial point: Refer to "Enlarged view of index mark".

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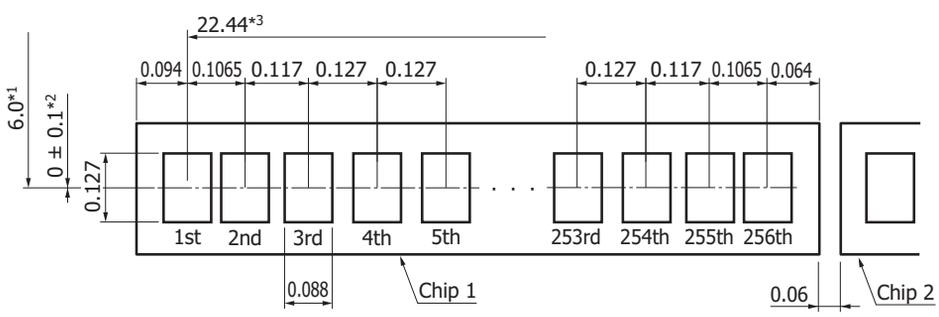
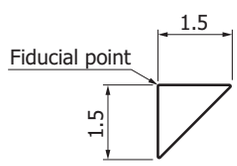
Enlarged view of chips (S11720-20, unit: mm)



*1: Distance from the fiducial point to photosensitive area center
*2: Variation for Y direction at pixel center
*3: Distance from the fiducial point to the first pixel center

KMPDC0728EA

Enlarged view of index mark (unit: mm)



KMPDC0729EA

Pin connections

S11720-20

Pin no.	Symbol	Description	I/O	Pin no.	Symbol	Description	I/O
1	CCLK	CMOS clock signal	I	31	Vss	Ground	-
2	CST	CMOS start signal	I	32	Vss	Ground	-
3	Vss	Ground	-	33	Vdd	Supply voltage (5 V)	I
4	CVG1	CMOS gain setting value switch 1	I	34	Vdd	Supply voltage (5 V)	I
5	CVG2	CMOS gain setting value switch 2	I	35	Vdd	Supply voltage (5 V)	I
6	SCLK	SPI clock signal	I	36	Vdd	Supply voltage (5 V)	I
7	SEN1	SPI enable signal (for ADC1)	I	37	Vss	Ground	-
8	SEN2	SPI enable signal (for ADC2)	I	38	Vss	Ground	-
9	SDIO	SPI input signal	I/O	39	Vss	Ground	-
10	RESET	ADC master reset	I	40	Vss	Ground	-
11	CLKOUT1	Pixel sync signal	O	41	Vss	Ground	-
12	CLKOUT2	Pixel sync signal	O	42	Vss	Ground	-
13	Vss	Ground	-	43	Vss	Ground	-
14	Vss	Ground	-	44	Vss	Ground	-
15	Out1[0]	Video output signal	O	45	Out2[7]	Video output signal	O
16	Vss	Ground	-	46	Vss	Ground	-
17	Out1[1]	Video output signal	O	47	Out2[6]	Video output signal	O
18	Vss	Ground	-	48	Vss	Ground	-
19	Out1[2]	Video output signal	O	49	Out2[5]	Video output signal	O
20	Vss	Ground	-	50	Vss	Ground	-
21	Out1[3]	Video output signal	O	51	Out2[4]	Video output signal	O
22	Vss	Ground	-	52	Vss	Ground	-
23	Out1[4]	Video output signal	O	53	Out2[3]	Video output signal	O
24	Vss	Ground	-	54	Vss	Ground	-
25	Out1[5]	Video output signal	O	55	Out2[2]	Video output signal	O
26	Vss	Ground	-	56	Vss	Ground	-
27	Out1[6]	Video output signal	O	57	Out2[1]	Video output signal	O
28	Vss	Ground	-	58	Vss	Ground	-
29	Out1[7]	Video output signal	O	59	Out2[0]	Video output signal	O
30	Vss	Ground	-	60	Vss	Ground	-

60-pin connector: DF12B-60DS-0.5 V (HIROSE ELECTRIC)

Note:

· To prevent signal deterioration, immediately after connecting the connector, connect digital buffers for capacitive load reduction to the video-output and pixel-sync signal terminals.

· The symbol of video output signal is defined as follows:

OutX[Y]

- X: 1 or 2: output ports
- Y: 0 to 7: Data bus bit

S11720-40

■ Connector 1

Pin no.	Symbol	Description	I/O	Pin no.	Symbol	Description	I/O
1	Vss	Ground	-	31	Vss	Ground	-
2	Out1[7]	Video output signal	O	32	Out2[0]	Video output signal	O
3	Vss	Ground	-	33	Vss	Ground	-
4	Out1[6]	Video output signal	O	34	Out2[1]	Video output signal	O
5	Vss	Ground	-	35	Vss	Ground	-
6	Out1[5]	Video output signal	O	36	Out2[2]	Video output signal	O
7	Vss	Ground	-	37	Vss	Ground	-
8	Out1[4]	Video output signal	O	38	Out2[3]	Video output signal	O
9	Vss	Ground	-	39	Vss	Ground	-
10	Out1[3]	Video output signal	O	40	Out2[4]	Video output signal	O
11	Vss	Ground	-	41	Vss	Ground	-
12	Out1[2]	Video output signal	O	42	Out2[5]	Video output signal	O
13	Vss	Ground	-	43	Vss	Ground	-
14	Out1[1]	Video output signal	O	44	Out2[6]	Video output signal	O
15	Vss	Ground	-	45	Vss	Ground	-
16	Out1[0]	Video output signal	O	46	Out2[7]	Video output signal	O
17	Vss	Ground	-	47	Vss	Ground	-
18	Vss	Ground	-	48	Vss	Ground	-
19	CLKOUT2	Pixel sync signal	O	49	Vss	Ground	-
20	CLKOUT1	Pixel sync signal	O	50	Vss	Ground	-
21	RESET	ADC master reset	I	51	Vss	Ground	-
22	SDIO	SPI input signal	I/O	52	Vss	Ground	-
23	SEN2	SPI enable signal (for ADC2)	I	53	Vss	Ground	-
24	SEN1	SPI enable signal (for ADC1)	I	54	Vss	Ground	-
25	SCLK	SPI clock signal	I	55	Vdd	Supply voltage (5 V)	I
26	CVG2	CMOS gain setting value switch 2	I	56	Vdd	Supply voltage (5 V)	I
27	CVG1	CMOS gain setting value switch 1	I	57	Vdd	Supply voltage (5 V)	I
28	Vss	Ground	-	58	Vdd	Supply voltage (5 V)	I
29	CST	CMOS start signal	I	59	Vss	Ground	-
30	CCLK	CMOS clock signal	I	60	Vss	Ground	-

60-pin connector: DY00-060S (KEL)

Note:

· To prevent signal deterioration, immediately after connecting the connector, connect digital buffers for capacitive load reduction to the video-output and pixel-sync signal terminals.

· The symbol of video output signal is defined as follows:

OutX[Y]

- X: 1 to 4: output ports
- Y: 0 to 7: Data bus bit

■ Connector 2

Pin no.	Symbol	Description	I/O	Pin no.	Symbol	Description	I/O
61	Vss	Ground	-	91	Vss	Ground	-
62	Out3[7]	Video output signal	O	92	Out4[0]	Video output signal	O
63	Vss	Ground	-	93	Vss	Ground	-
64	Out3[6]	Video output signal	O	94	Out4[1]	Video output signal	O
65	Vss	Ground	-	95	Vss	Ground	-
66	Out3[5]	Video output signal	O	96	Out4[2]	Video output signal	O
67	Vss	Ground	-	97	Vss	Ground	-
68	Out3[4]	Video output signal	O	98	Out4[3]	Video output signal	O
69	Vss	Ground	-	99	Vss	Ground	-
70	Out3[3]	Video output signal	O	100	Out4[4]	Video output signal	O
71	Vss	Ground	-	101	Vss	Ground	-
72	Out3[2]	Video output signal	O	102	Out4[5]	Video output signal	O
73	Vss	Ground	-	103	Vss	Ground	-
74	Out3[1]	Video output signal	O	104	Out4[6]	Video output signal	O
75	Vss	Ground	-	105	Vss	Ground	-
76	Out3[0]	Video output signal	O	106	Out4[7]	Video output signal	O
77	Vss	Ground	-	107	Vss	Ground	-
78	Vss	Ground	-	108	Vss	Ground	-
79	CLKOUT4	Pixel sync signal	O	109	Vss	Ground	-
80	CLKOUT3	Pixel sync signal	O	110	Vss	Ground	-
81	RESET	ADC master reset	I	111	Vss	Ground	-
82	SDIO	SPI input signal	I/O	112	Vss	Ground	-
83	SEN4	SPI enable signal (for ADC4)	I	113	Vss	Ground	-
84	SEN3	SPI enable signal (for ADC3)	I	114	Vss	Ground	-
85	SCLK	SPI clock signal	I	115	Vdd	Supply voltage (5 V)	I
86	CVG2	CMOS gain setting value switch 2	I	116	Vdd	Supply voltage (5 V)	I
87	CVG1	CMOS gain setting value switch 1	I	117	Vdd	Supply voltage (5 V)	I
88	Vss	Ground	-	118	Vdd	Supply voltage (5 V)	I
89	CST	CMOS start signal	I	119	Vss	Ground	-
90	CCLK	CMOS clock signal	I	120	Vss	Ground	-

60-pin connector: DY00-060S (KEL)

Note:

· To prevent signal deterioration, immediately after connecting the connector, connect digital buffers for capacitive load reduction to the video-output and pixel-sync signal terminals.

· The symbol of video output signal is defined as follows:

OutX[Y]

- X: 1 to 4: output ports
- Y: 0 to 7: Data bus bit

Precautions

(1) Electrostatic countermeasures
This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools. Also protect this device from surge voltages which might be caused by peripheral equipment.

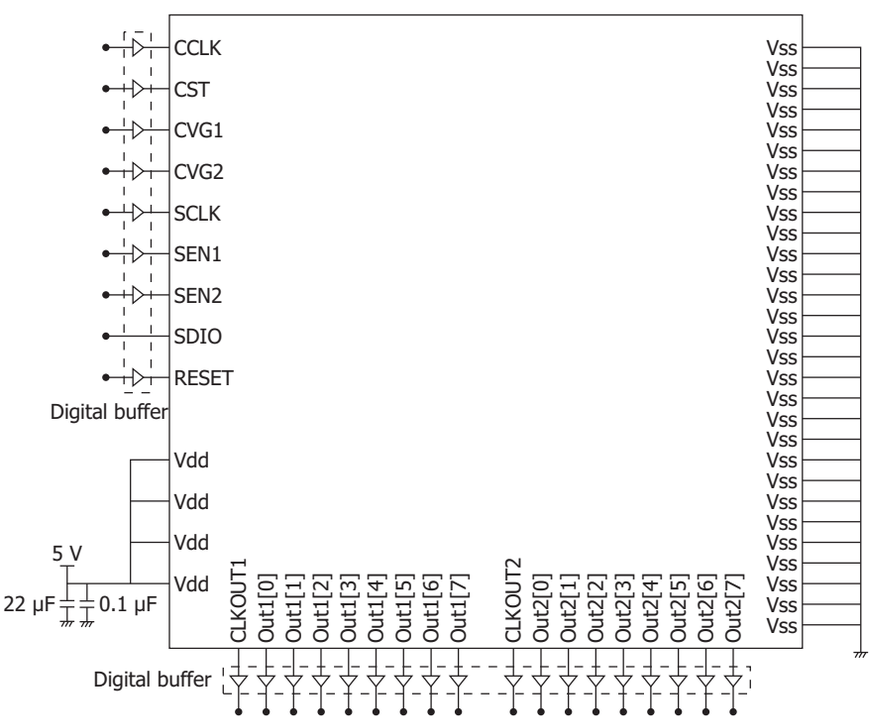
(2) Protective Resin
If dust or stain adheres to the surface of the protective resin, it will appear as black spots on the image. To remove dust, apply an air blower. If greasy smudges adhere to it, avoid scratching and then gently wipe them away with a cotton swab or the like moistened with ethyl alcohol. Vigorously rubbing or frequently wiping it may reduce the electrical and optical characteristics, and reduce their reliability.

(3) Operating and storage environments
Handle the device within the temperature range of the absolute maximum ratings. Operating or storing the device at an excessively high temperature and humidity may cause variations in performance characteristics and must be avoided.

(4) UV light irradiation
Because this product is not designed to resist characteristic deterioration under UV light irradiation, do not apply UV light irradiation to it.

Connection circuit example

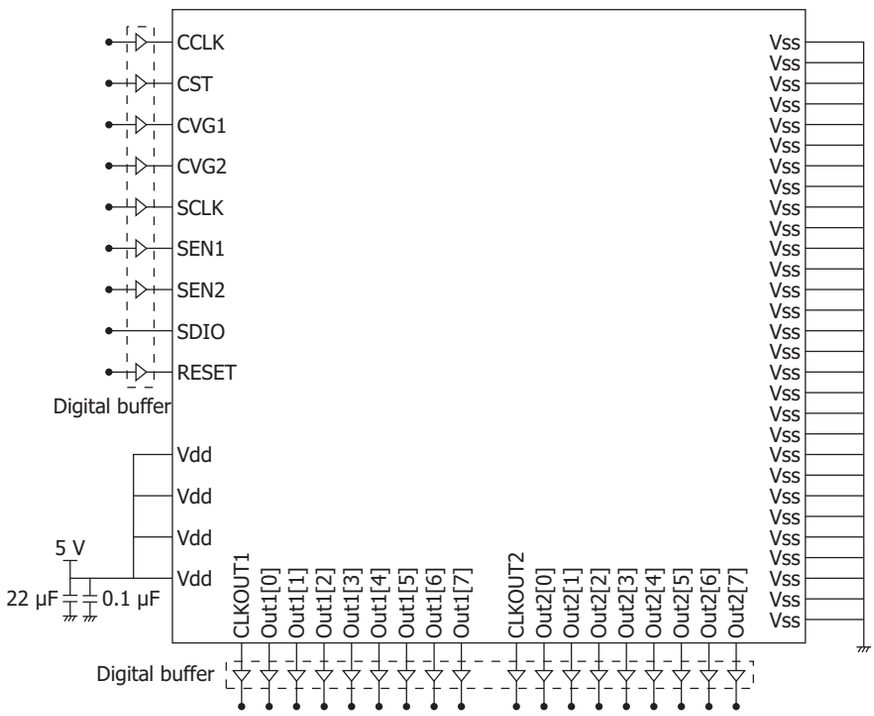
S11720-20



KMPDC0719EB

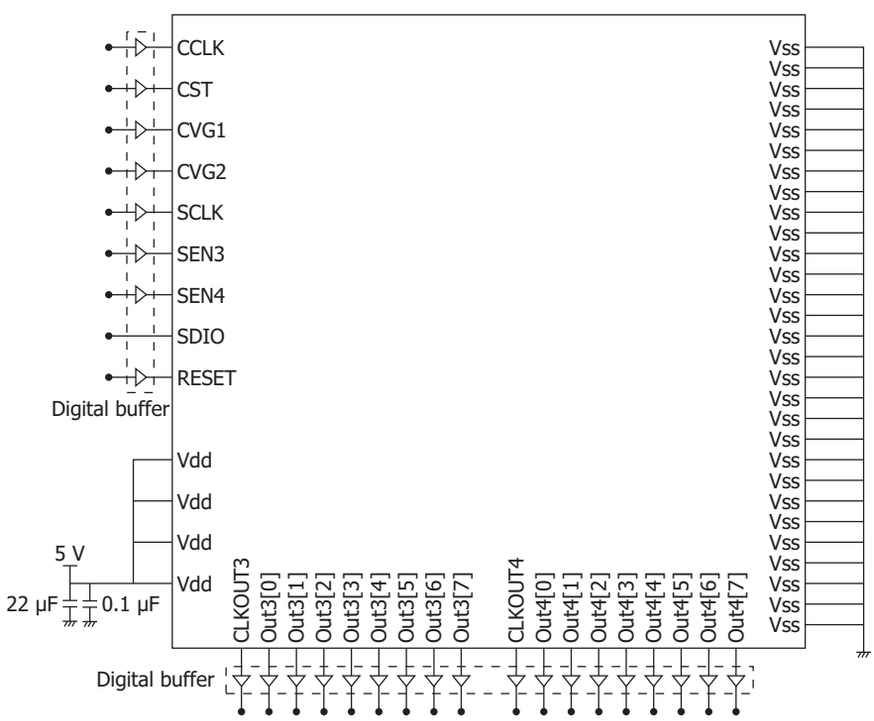
S11720-40

■ Connector 1 [Refer to "Dimensional outline" (P.14)]



KMPDC0719EB

■ Connector 2 [Refer to "Dimensional outline" (P.14)]



KMPDC0720EB

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

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