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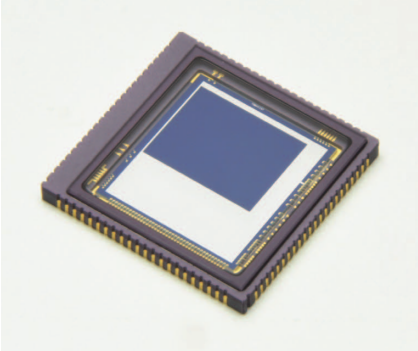
NEW

CMOS area image sensor



S14501

Visible/near infrared high sensitivity, back-illuminated APS (active pixel sensor) type

The S14501 is a back-illuminated APS type CMOS area image sensor that has high sensitivity in the visible to near infrared region. The pixel format is SXGA (1280 × 1024 pixels). In addition, imaging is possible at a maximum rate of 146 frames/s.
It is an all-digital I/O type with built-in timing generator, bias generator, amplifiers, and A/D converters. Rolling shutter readout or global shutter readout can be selected. Since the number of readout pixels in the vertical direction can be changed as you like, high-speed readout is possible according to the number of pixels.

Features

- **Pixel size: 7.4 × 7.4 µm**
- **Number of pixels: 1280 × 1024 (SXGA)**
- **High-speed readout: 146 frames/s max.**
- **SPI communication function (partial readout, gain switching, frame start mode selection, etc.)**
- **Rolling/global shutter readout**

Applications

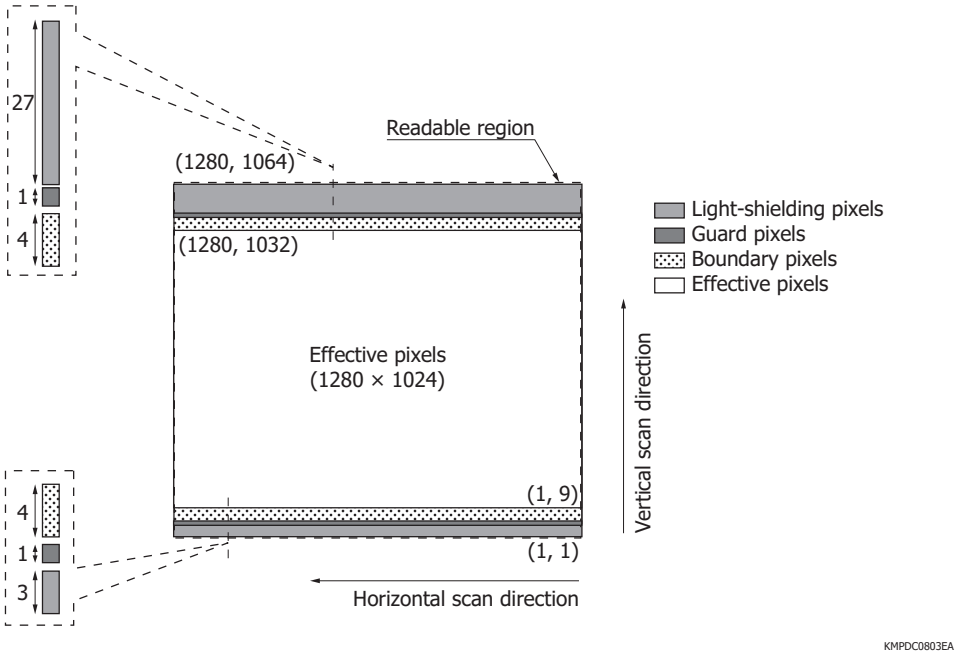
- **Machine vision**
- **Tracking**
- **Security (infrared camera)**
- **Position and shape recognition of infrared light spot**

Structure

Parameter	Specification	Unit
Image size (H × V)	9.472 × 7.578	mm
Pixel size	7.4 × 7.4	µm
Pixel pitch	7.4	µm
Total number of pixels (H × V)	1280 × 1064	pixels
Number of effective pixels (H × V)	1280 × 1024	pixels
Boundary pixels*1	Top 4 and bottom 4 rows outside the effective pixel area	-
Guard pixels*2	Rows 4 and 1037	
Light-shielding pixels*3	Rows 1 to 3 and rows 1038 to 1064	
Package	Ceramic	-
Window material	Borosilicate glass	-

*1: Same pixels as the effective pixels
*2: Pixels with a fixed photodiode potential
*3: Pixels whose photodiode is shielded with metal

Pixel layout



Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Condition	Value	Unit
Supply voltage	Analog terminal	Vdd(A)		-0.3 to +3.9	V
	Digital terminal	Vdd(D)		-0.3 to +3.9	
	Counter terminal	Vdd(C)		-0.3 to +3.9	
Digital input signal terminal voltage*4		Vi		-0.3 to +3.9	V
Vref_cp1 terminal voltage*5		Vref_cp1		-0.3 to +6.5	V
Vref_cp2 terminal voltage*6		Vref_cp2		-2.0 to +0.3	V
Operating temperature		Topr	No dew condensation*7	-40 to +60	°C
Storage temperature		Tstg	No dew condensation*7	-40 to +60	°C
Reflow soldering conditions*8		Tsol		Peak temperature: 260 °C, 3 times (see P.13)	-

*4: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_reset, PLL-reset, MST
*5: There is no need to supply voltage externally because voltage is generated inside the chip. To reduce noise, insert a capacitor around 1 µF between each terminal and GND.
*6: Voltage is generated inside the chip, but apply an external bias voltage (-1.5 V, 2 mA) to improve the image quality. To reduce noise, insert a capacitor around 1 µF between each terminal and GND.
*7: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*8: JEDEC level 2a
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended operating conditions (Ta=25 °C)

Input voltage

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog terminal	Vdd(A)	3.0	3.3	3.6	V
	Digital terminal	Vdd(D)	3.0	Vdd(A)	3.6	
	Counter terminal	Vdd(C)	2.4	2.5	2.6	
Digital input voltage*9	High level	Vi(H)	Vdd(D) - 0.25	Vdd(D)	Vdd(D) + 0.25	V
	Low level	Vi(L)	0	-	0.25	
Vref_cp2 terminal voltage		Vref_cp2	-2.0	-1.5	-1.0	V

*9: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_reset, PLL_reset, MST

Digital input signal

[Recommended operating conditions (input voltage) Typ. value]*10

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master clock pulse frequency	f(MCLK)	25	30	35	MHz
Master clock pulse duty cycle	D(MCLK)	45	50	55	%
SPI clock pulse frequency	f(SPI_SCLK)	-	-	10	MHz
Rise time*11	tr(sigi)	-	5	7	ns
Fall time*11	tf(sigi)	-	5	7	ns

*10: SPI_CS, SPI_SCLK, SPI_MOSI, SPI_RSTB, MCLK, TG_reset, PLL-reset, MST
*11: Time for the input voltage to rise or fall between 10% and 90%

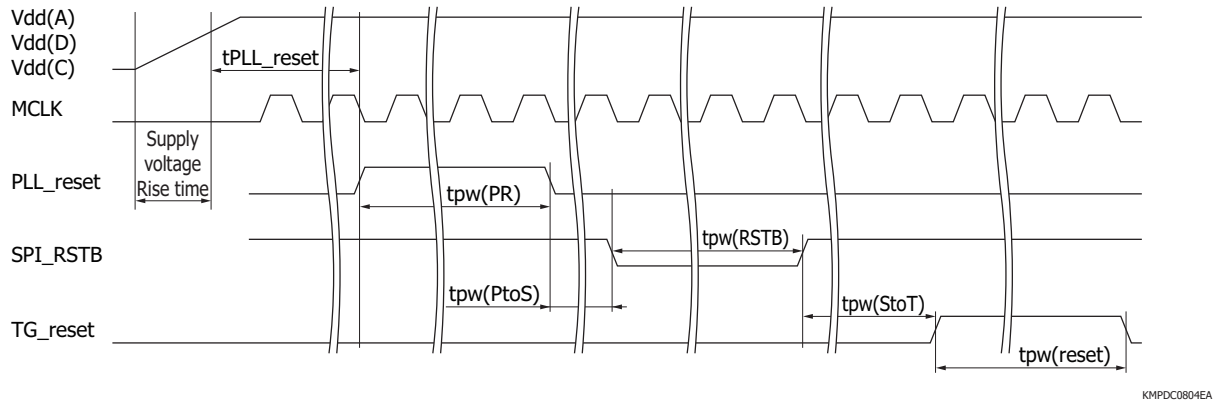
Reset signal (at power-on)

[Recommended operating conditions (input voltage) Typ. value]

Parameter	Symbol	Min.	Typ.	Max.	Unit
tPLL_reset standby time	tPLL_reset	1	-	-	µs
tPLL_reset high period	tpw(PR)	100	-	-	ns
tPLL_reset-SPI_RSTB period	tpw(PtoS)	100	-	-	ns
SPI_RSTB low period	tpw(RSTB)	100	-	-	ns
SPI_RSTB-TG_reset period	tpw(StoT)	100	-	-	ns
TG_reset high period*12	tpw(reset)	3	-	-	cycles

*12: If you input a Reset signal, correct data cannot be obtained in the frame immediately after input. Therefore, use the data of the second frame or later.
One cycle is the period of a single master clock pulse cycle.

■ Reset signal input timing



Note: At power-on, input the SPI_RSTB and Reset signals at the timings shown in the figure above to initialize the timing circuit and SPI circuit after all the supply voltages have risen to the recommended operating conditions [Vdd (A)=Vdd (D)=3.0 V, Vdd (C)=2.4 V].

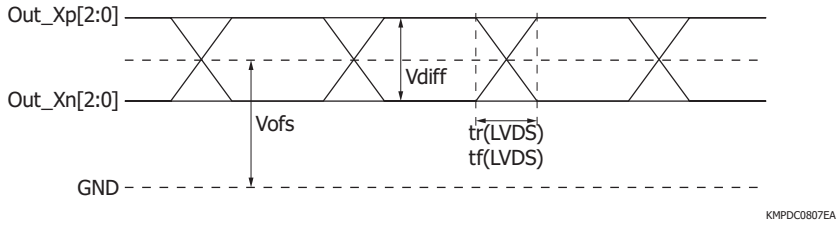
Electrical characteristics [Ta=25 °C, recommended operating conditions (input voltage, digital input signal) Typ. value (P.3)]

Digital output signal

Parameter		Symbol	Min.	Typ.	Max.	Unit
Video data rate (per port)		VR		f(MCLK) × 2*13		Hz
Pixel sync signal (pclk) frequency		f(pclk)		f(MCLK) × 8		Hz
Digital output voltage (LVDS output)*13 *14	Offset	Vofs	1.13	1.25	1.38	V
	Differential	Vdiff	0.25	0.35	0.45	
Rise time (LVDS output)*13 *14 *15		tr(LVDS)	-	2	3	ns
Fall time (LVDS output)*13 *14 *15		tf(LVDS)	-	2	3	ns
Delay between pixel output sync signal and video output		tPDD	-	-	3	ns
Delay between pixel output sync signal and line sync signal	Rise time	tPDHR	-	-	3	ns
	Fall time	tPDHF	-	-	3	
Delay between pixel output sync signal and frame sync signal	Rise time	tPDVR	-	-	3	ns
	Fall time	tPDVF	-	-	3	
Delay between pixel output sync signal and deserialization sync signal	Rise time	tPDCR	-	-	3	ns
	Fall time	tPDCF	-	-	3	
Digital output voltage (CMOS output)*16	High	Vsigo(H)	Vdd(D) - 0.25	Vdd(D)	-	V
	Low	Vsigo(L)	-	0	0.25	
Rise time (CMOS output)*16 *17		tr(sigo)	-	10	12	ns
Fall time (CMOS output)*16 *17		tf(sigo)	-	10	12	ns

*13: When 100 Ω is connected across the LVDS output terminals.
*14: Pixel sync signal (pclk), line sync signal (Hsync), frame sync signal (Vsync), parallelization signal (CTR), pixel output (OutA to OutE)
*15: Time for the output voltage to rise or fall between 10% and 90% when there is a 2 pF load capacitor attached to the output terminal.
*16: SPI_MISO
*17: Time for the output voltage to rise or fall between 10% and 90% when there is a 10 pF load capacitor attached to the output terminal.

■ LVDS output voltage



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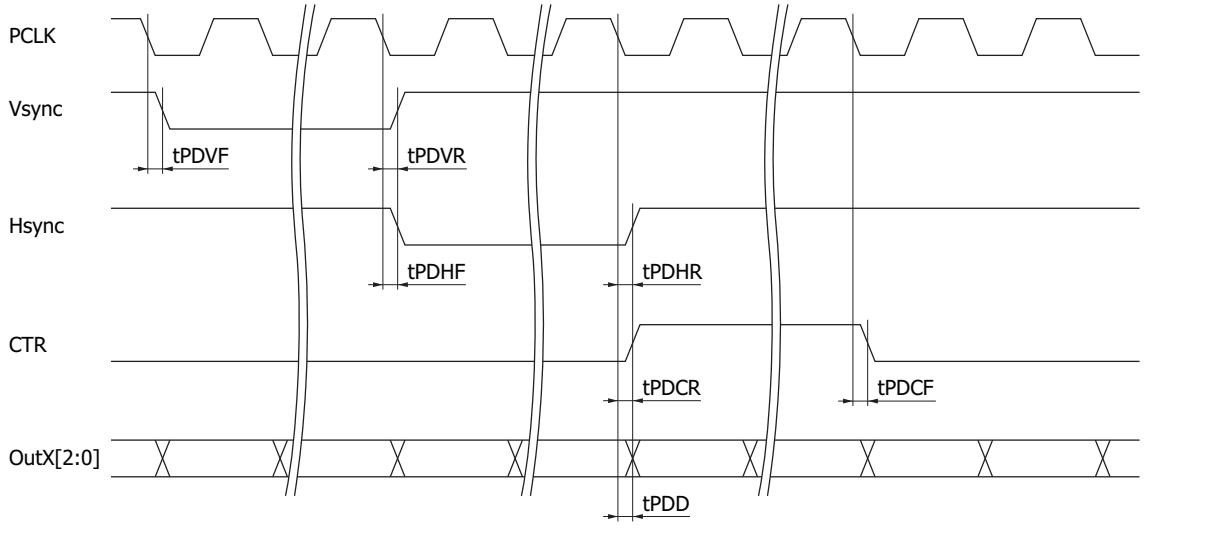
■ Sync signal, video signal



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Current consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit
Total of analog terminal and digital terminal*18	I1	-	280	380	mA
Counter terminal*18	I2	-	210	330	

*18: Dark state, master clock pulse frequency=30 MHz, high-speed mode, load capacitance of each output terminal= 5 pF

A/D converter

■ High resolution mode (SPI value: DAC_N=3, TG_N=19)

Parameter	Symbol	Specification	Unit
Resolution	Reso	12	bit
Conversion frequency	fcon	30	kHz
A/D resolution	-	0.31	mV/DN

■ High-speed mode (SPI setting: DAC_N=0, TG_N=3)

Parameter	Symbol	Specification	Unit
Resolution	Reso	10	bit
Conversion frequency	fcon	150	kHz
A/D resolution	-	1.25	mV/DN

Electrical and optical characteristics

[Ta=25 °C, recommended operating conditions (input voltage, digital input signal) Typ. value, MCLK=30 MHz, Gain: default value, offset: default value, rolling shutter]

Common to all modes

Parameter			Symbol	Min.	Typ.	Max.	Unit
Spectral response range			λ	400 to 1100			nm
Peak sensitivity wavelength			λp	-	660	-	nm
Photoresponse nonuniformity*19			PRNU	-	-	4	%
Defective pixels	Point defect	White spot*20	WS	-	-	10	pixels
		Black spot*21	BS	-	-	10	pixels
	Cluster defect*22		ClsD	-	-	0	pcs

*19: Output nonuniformity when white uniform light at approximately 50% saturation is applied. It is calculated excluding boundary pixels, guard pixels, light-shielding pixels, and defective pixels and is defined as follows:
PRNU = (ΔX/X) × 100 [%]
ΔX: standard deviation, X: average output of all pixels

*20: Pixels whose dark output exceeds 3600 DN/s when gain=1 in rolling shutter mode (excluding boundary pixels and guard pixels)

*21: Pixels whose output value is 50% or less than that of adjacent pixels when uniform white light is applied at approximately 50% the saturation level (excluding boundary pixels, guard pixels, and light-shielding pixels)

*22: Point defect spanning two or more consecutive pixels

High resolution mode

■ Global shutter mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
Offset output*23	Vo	0	200	400	DN
Offset variation*24	DSNU	-	15	100	DN rms
Dark output*23	DS	-	30	600	DN/s
Saturation exposure*25	Lsat	-	0.13	-	lx·s
Photosensitivity*25	Sw	14000	18000	-	DN/lx·s
Saturation output*26	Vsat	1600	2300	-	DN
Random noise*23	RN	-	5	8	DN rms
Dynamic range*27	DR	46	53	-	dB
Conversion factor	-	-	37	-	μV/e$^-$
	-	-	0.119	-	DN/e$^-$

■ Rolling shutter mode

Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Offset output*23	Vo	1	0	200	400	DN
		2	100	200	400	
		8	100	200	400	
Offset variation*24	DSNU	1	-	3	10	DN rms
		2	-	3	15	
		8	-	3	15	
Dark output*23	DS	1	-	30	600	DN/s
		2	-	60	1200	
		8	-	240	4800	
Saturation exposure*25	Lsat	1	-	0.19	-	lx·s
		2	-	0.10	-	
		8	-	0.02	-	
Photosensitivity*25	Sw	1	14000	18000	-	DN/lx·s
		2	28000	36000	-	
		8	112000	144000	-	
Saturation output*26	Vsat	1	3000	3500	-	DN
		2	3000	3500	-	
		8	3000	3500	-	
Random noise*23	RN	1	-	1.7	3.4	DN rms
		2	-	2	4	
		8	-	5.2	8	
Dynamic range*27	DR	1	59	66	-	dB
		2	58	65	-	
		8	51	57	-	
Conversion factor		1	-	37	-	μV/e$^-$
			-	0.119	-	DN/e$^-$
		2	-	74	-	μV/e$^-$
			-	0.238	-	DN/e$^-$
		8	-	280	-	μV/e$^-$
			-	0.952	-	DN/e$^-$

*23: Average output of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*24: Standard deviation of output values of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*25: λ=555 nm
*26: Average of the values obtained by subtracting the offset output from the output values when light equivalent to twice the saturation exposure is applied (excluding boundary pixels, guard pixels, light-shielding pixels, and defective pixels)
*27: Ratio of saturation output to random noise
Note: DN (digital number): unit of A/D converter output

High-speed mode

■ Global shutter mode

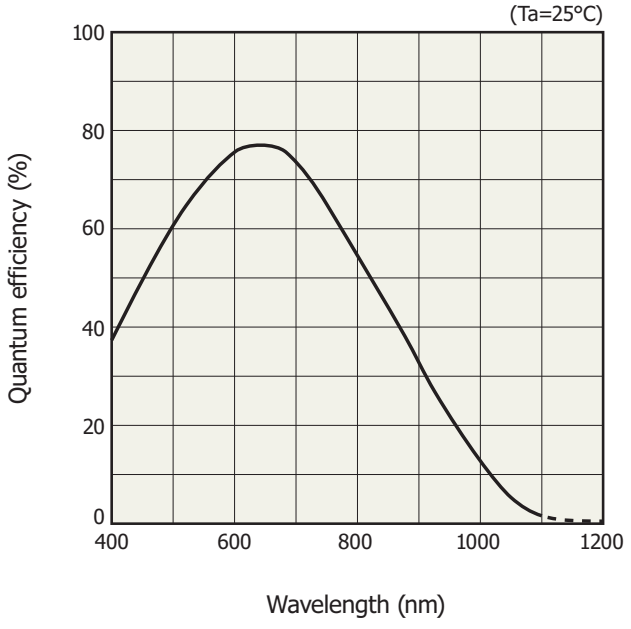
Parameter	Symbol	Min.	Typ.	Max.	Unit
Offset output*23	Vo	0	200	400	DN
Offset variation*24	DSNU	-	15	100	DN rms
Dark output*23	DS	-	8	150	DN/s
Saturation exposure*25	Lsat	-	0.16	-	lx·s
Photosensitivity*25	Sw	3500	4500	-	DN/lx·s
Saturation output*26	Vsat	600	700	-	DN
Random noise*23	RN	-	1.5	2.2	DN rms
Dynamic range*27	DR	46	53	-	dB
Conversion factor	-	-	37	-	μV/e⁻
	-	-	0.03	-	DN/e⁻

■ Rolling shutter mode

Parameter	Symbol	Gain	Min.	Typ.	Max.	Unit
Offset output*23	Vo	1	0	200	400	DN
		2	0	200	400	
		8	0	200	400	
Offset variation*24	DSNU	1	-	3	10	DN rms
		2	-	3	15	
		8	-	3	15	
Dark output*23	DS	1	-	8	150	DN/s
		2	-	16	300	
		8	-	64	1200	
Saturation exposure*25	Lsat	1	-	0.16	-	lx·s
		2	-	0.08	-	
		8	-	0.02	-	
Photosensitivity*25	Sw	1	3500	4500	-	DN/lx·s
		2	7000	9000	-	
		8	21000	36000	-	
Saturation output*26	Vsat	1	600	700	-	DN
		2	600	700	-	
		8	600	700	-	
Random noise*23	RN	1	-	0.7	1.4	DN rms
		2	-	0.7	1.4	
		8	-	1.4	2.1	
Dynamic range*27	DR	1	53	60	-	dB
		2	53	60	-	
		8	49	54	-	
Conversion factor		1	-	37	-	μV/e⁻
			-	0.03	-	DN/e⁻
		2	-	74	-	μV/e⁻
			-	0.059	-	DN/e⁻
		8	-	280	-	μV/e⁻
			-	0.237	-	DN/e⁻

*23: Average output of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*24: Standard deviation of output values of all pixels excluding boundary pixels, guard pixels, and defective pixels under light-shielded condition
*25: λ=555 nm
*26: Average of the output values (excluding boundary pixels, guard pixels, light-shielding pixels, and defective pixels) when light equivalent to twice the saturation exposure is applied but with the offset output subtracted
*27: Ratio of saturation output to random noise
Note: DN (digital number): unit of A/D converter output

Spectral response (typical example)



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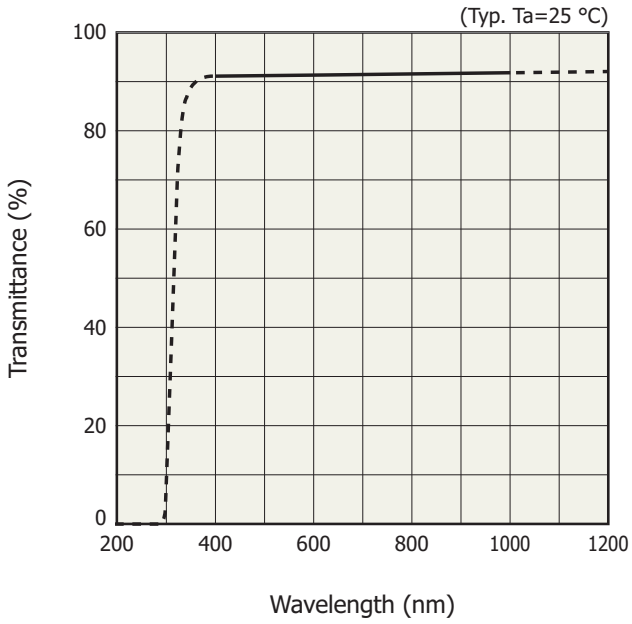
Spectral transmittance of window material



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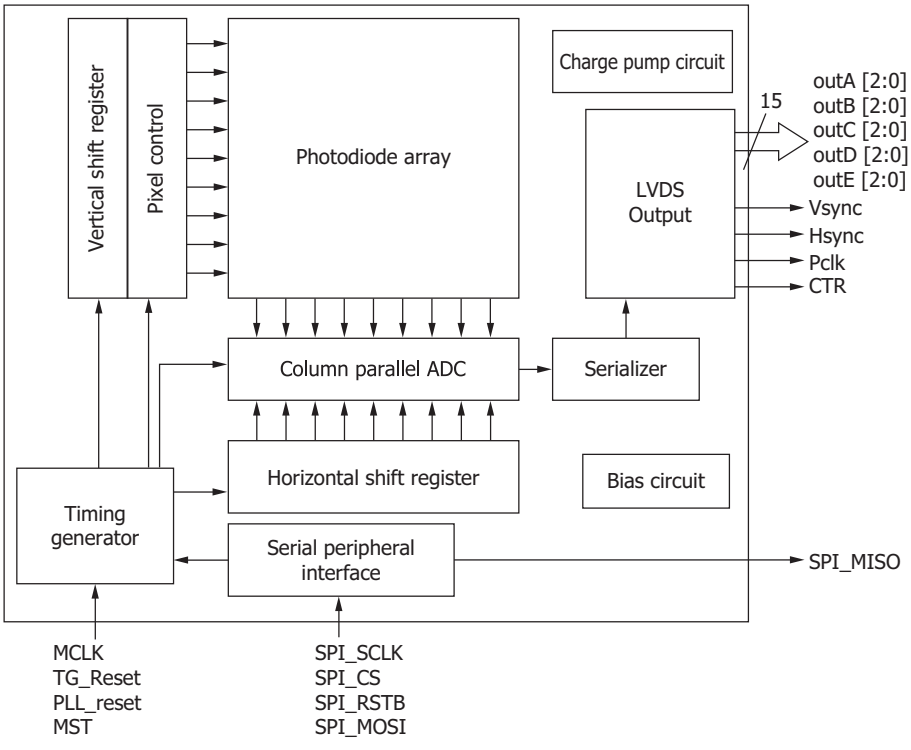
Block diagram



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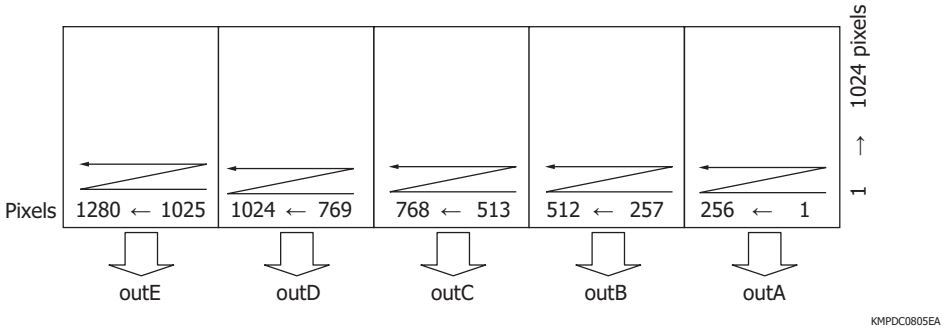
Port assignment

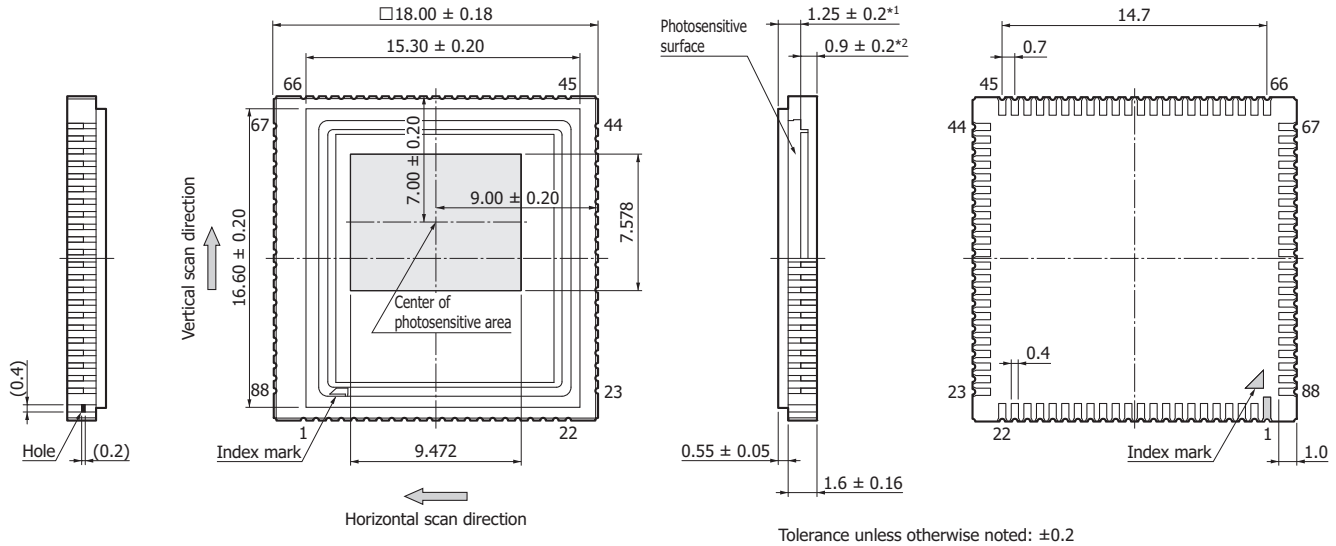


Setting using the SPI and the like

The following parameters can be set using the serial peripheral interface (SPI). However, use MST (external input signal) to set the integration time and blanking period in external start mode.

Parameter	Mode and explanation	
Shutter mode (Default: rolling shutter mode)	Rolling shutter mode	Rolling shutter mode is advantageous in that readout noise is small because readout is performed through the CDS circuit. However, the disadvantage is that the integration start/end timing is different for each row.
	Global shutter mode	Global shutter mode is advantageous in that the integration start/end timing is the same for all pixels. However, the disadvantage is that the readout noise is large because a CDS circuit is not used.
Frame start mode (Default: internal start pulse mode)	Internal start pulse mode	Readout starts automatically when the power is turned on. The frame period is determined by the number of readout rows and line rate.
	External start pulse mode	Readout starts when the rising edge of MST is detected. MST is also used to control the integration time. The low period of MST is roughly the integration time.
Integration time	Internal start pulse mode	Integration time is set using SPI.
	External start pulse mode	Integration time is set using MST.
Blanking period	Internal start pulse mode	Blanking period is set for 0 to 16797215 rows using SPI.
	External start pulse mode	Blanking period is from the end of a readout to the rising edge of the next MST.
Readout region	The readout region can be set at the pixel level. A single readout region can be set in each frame.	
Output gain (rolling shutter mode only)	The gain can be set to 1x, 2x, or 8x.	
Output offset	The output offset value can be adjusted. The default output level is approximately 200 DN.	
Line rate (Default: high resolution mode)	High resolution mode	The default line rate. The resolution is 12-bit.
	High-speed mode	9.4-bit resolution (data width: 10-bit).

Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.2
Angle accuracy of photosensitive area: -2°≤θ≤2°
Weight: 1.64 g
*1: Distance from glass surface to photosensitive surface
*2: Distance from package bottom to photosensitive surface

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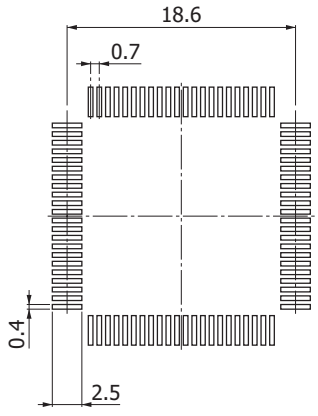
Note: There is a hole on the side of this product that allows outside air to enter the package to prevent condensation. Do not wash the product by soaking in cleaning solution, as the solution will enter the package and may cause problems.

Recommended land pattern (unit: mm)



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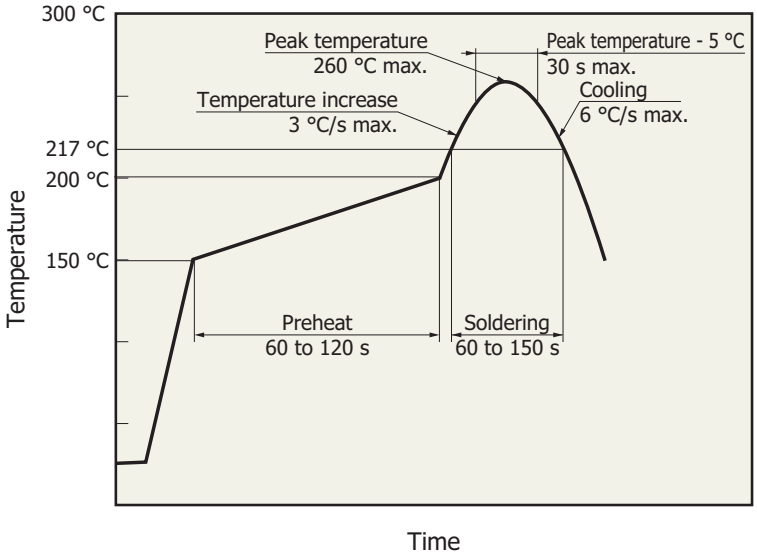
Pin connections

Pin no.	Symbol	Description	I/O
1	LVDS_outAp[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
2	LVDS_outAn[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
3	LVDS_outAp[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
4	LVDS_outAn[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
5	LVDS_outAp[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
6	GND	Ground	I
7	Vdd(D)*29 *31	Digital supply voltage	I
8	GND	Ground	I
9	Vdd(C)*29 *31	Counter supply voltage	I
10	LVDS_pclkn*28	Pixel sync signal	O
11	LVDS_pclkp*28	Pixel sync signal	O
12	LVDS_Hsyncn*28	Line (horizontal) sync signal	O
13	LVDS_Hsyncp*28	Line (horizontal) sync signal	O
14	LVDS_Vsyncn*28	Frame (vertical) sync signal	O
15	LVDS_Vsyncp*28	Frame (vertical) sync signal	O
16	LVDS_CTRn*28	4-bit serializer sync signal	O
17	LVDS_CTRp*28	4-bit serializer sync signal	O
18	Vref3*30 *32	Bias voltage for LVDS	O
19	Vref2*30 *32	Bias voltage for LVDS	O
20	Vref1*30 *32	Bias voltage for LVDS	O
21	GND	Ground	I
22	Vdd(D)*29 *31	Digital supply voltage	I
23	GND	Ground	I
24	Vdd(A)*29 *31	Analog supply voltage	I
25	SPI_RSTB	SPI reset signal	I
26	SPI_MOSI	SPI input signal	I
27	SPI_CS	SPI selection signal	I
28	SPI_SCLK	SPI clock signal	I
29	TG_RESET	Timing generator reset	I
30	MCLK	Master clock signal (30 MHz recommended)	I
31	PLL_reset	PLL circuit reset	I
32	MST	Master start signal	I
33	SPI_MISO	SPI output signal	O
34	GND	Ground	I
35	GND	Ground	I
36	GND	Ground	I
37	Vref_cp2*33	Supply voltage for pixels	I
38	GND	Ground	I
39	NC*34	No connection	-
40	Vref10*30 *32	Bias voltage for amplifier	O
41	Vref9*30 *32	Bias voltage for LVDS	O
42	Vref8*30 *32	Bias voltage for amplifier	O
43	Vref7*30 *32	Bias voltage for A/D converter	O
44	Vref6*30 *32	Bias voltage for A/D converter	O
45	GND	Ground	I

Pin no.	Symbol	Description	I/O
46	Vref_cp1*30 *35	Bias voltage for charge pump circuit	I
47	Vref_cp2*33	Supply voltage for pixels	I
48	GND	Ground	I
49	Vdd(A)*29 *31	Analog supply voltage	I
50	Vdd(A)*29 *31	Analog supply voltage	I
51	GND	Ground	I
52	Vdd(A)*29 *31	Analog supply voltage	I
53	Vref5*30 *32	Bias voltage for amplifier	O
54	Vref4*30 *32	Bias voltage for amplifier	O
55	NC*34	No connection	-
56	Vdd(D)*29 *31	Digital supply voltage	I
57	GND	Ground	I
58	Vdd(C)*29 *31	Counter supply voltage	I
59	GND	Ground	I
60	Vdd(D)*29 *31	Digital supply voltage	I
61	GND	Ground	I
62	LVDS_outEn[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
63	LVDS_outEp[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
64	LVDS_outEn[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
65	LVDS_outEp[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
66	LVDS_outEn[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
67	LVDS_outEp[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
68	LVDS_outDn[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
69	LVDS_outDp[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
70	LVDS_outDn[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
71	LVDS_outDp[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
72	LVDS_outDn[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
73	LVDS_outDp[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
74	LVDS_outCn[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
75	LVDS_outCp[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
76	LVDS_outCn[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
77	LVDS_outCp[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
78	LVDS_outCn[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
79	LVDS_outCp[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
80	GND	Ground	I
81	Vdd(C)*29 *31	Counter supply voltage	I
82	LVDS_outBn[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
83	LVDS_outBp[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O
84	LVDS_outBn[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
85	LVDS_outBp[1]*28	Pixel output, LVDS (4, 5, 6, 7-bit) signal	O
86	LVDS_outBn[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
87	LVDS_outBp[0]*28	Pixel output, LVDS (0, 1, 2, 3-bit) signal	O
88	LVDS_outAn[2]*28	Pixel output, LVDS (8, 9, 10, 11-bit) signal	O

*28: LVDS output. Terminate across the LVDS output wires with a 100 Ω resistor.
*29: To reduce noise, insert 0.1 µF and 22 µF capacitors between each terminal and GND.
*30: To reduce noise, insert a capacitor around 1 µF between each terminal and GND.
*31: Apply voltage to all supply voltage terminals.
*32: A terminal for monitoring the bias voltage generated inside the chip.
*33: Voltage is generated inside the chip, but apply an external bias voltage -1.5 V (which can supply 2 mA) to improve the image quality.
*34: Leave NC pins open; do not connect to GND.
*35: Be sure to insert the diode so that Vdd(A) is on the anode side and pin 46 is on the cathode side.

Recommended reflow soldering conditions (typical example)



· This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 72 hours.
· The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. When you set reflow soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.

Recommended baking conditions

See precautions (surface mount type products).

Precautions

(1) Electrostatic countermeasures
This device has a built-in protection circuit against static electrical charges. However, to prevent destroying the device with electrostatic charges, take countermeasures such as grounding yourself, the workbench and tools to prevent static discharges. Also protect this device from surge voltages which might be caused by peripheral equipment.

(2) Input window
If dust or stain adheres to the surface of the input window glass, it will appear as black spots on the image. When cleaning, avoid rubbing the window surface with dry cloth, dry cotton swab or the like, since doing so may generate static electricity. Use a piece of soft cloth, a cotton swab, or the like moistened with alcohol to wipe dust and stain off the window surface. Then blow compressed air onto the window surface so that no spots remain.

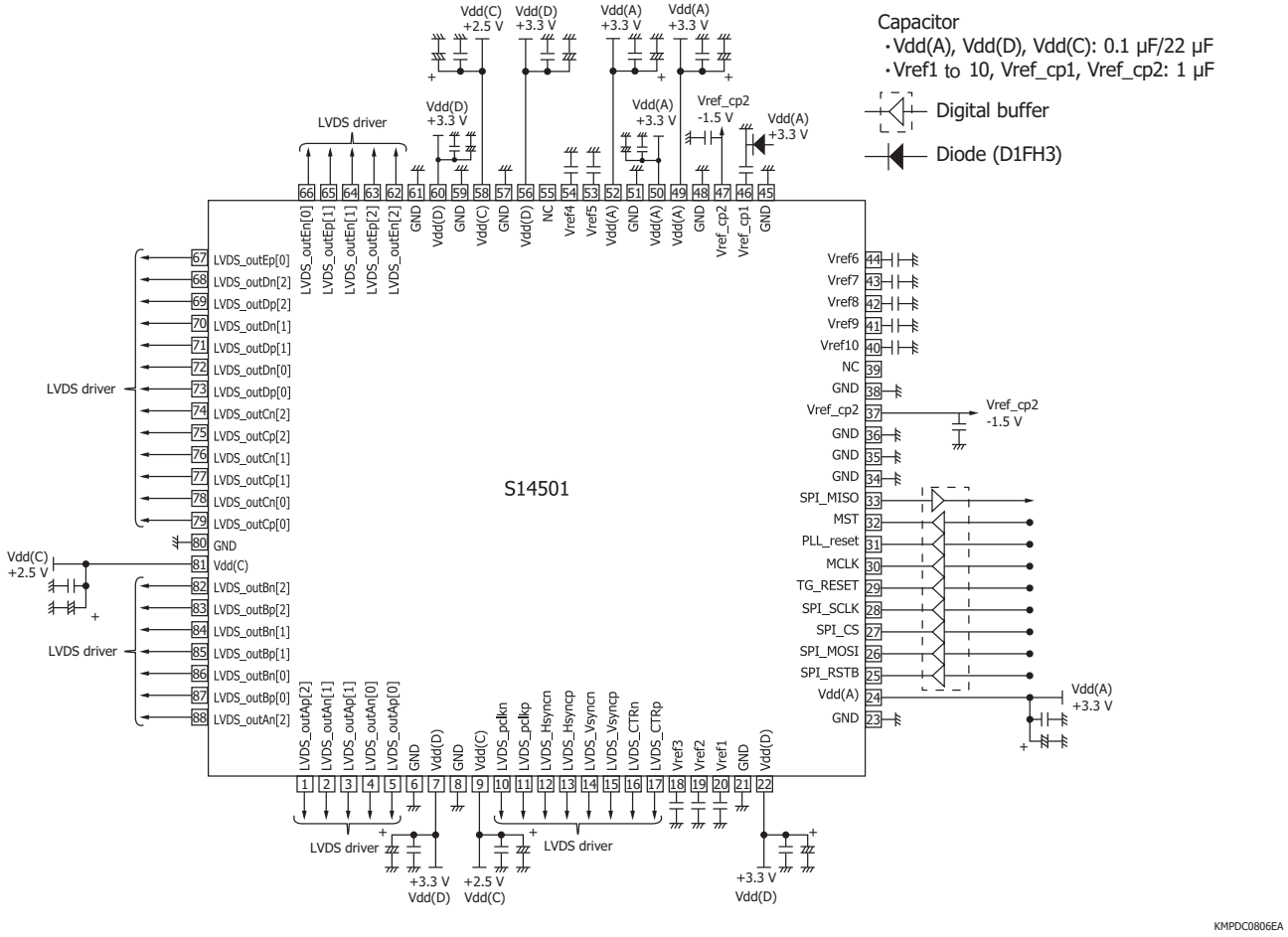
(3) Soldering
To prevent damaging the device during soldering, take precautions to prevent excessive soldering temperatures and times. Soldering should be performed within 5 seconds at a soldering temperature below 260 °C.

(4) Reflow soldering
Soldering conditions vary depending on the size of the circuit board, reflow oven, and the like. Check the conditions advance before soldering. Note that the bonding portion between the ceramic base and the glass may discolor after reflow soldering, but this has no adverse effects on the hermetic sealing of the product.

(5) UV light irradiation
This product is not designed to resist characteristic deterioration under UV light irradiation. Do not apply UV light to it.

(6) Cleaning
There is a hole on the side of this product that allows outside air to enter the package to prevent condensation. Do not wash the product by soaking in cleaning solution, as the solution will enter the package and may cause problems.

Connection circuit example



Note: Leave NC pins open; do not connect to GND.

Related information

www.hamamatsu.com/sp/ssd/doc_ja.html

■ Precautions
· Disclaimer
· Image sensors
· Surface mount type products

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