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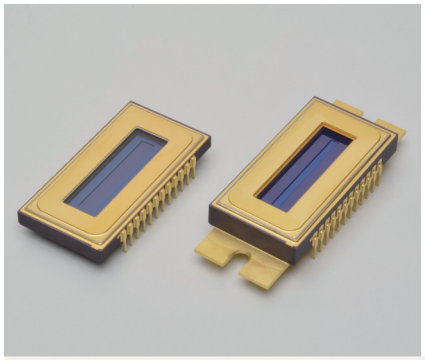
NEW

CCD area image sensor



S13240/S13241 series
S10140/S10141 series (-01)

Low readout noise, high resolution (pixel size: 12 µm)

The S13240/S13241 series and S10140/S10141 series (-01) are back-thinned FFT-CCD area image sensors developed for low-light-level detection. By using the binning operation, they can be used as a linear image sensor having a vertically long photosensitive area. This makes them suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. These products feature low noise and low dark current (MPP mode operation). This allows low-light-level detection by making the integration time longer. And, wide dynamic range has been achieved by increasing the saturation charge than that of the previous product (S10140/S10141 series).
The S13240/S13241 series is a high-speed readout type, and the S10140/S10141 series (-01) is a low noise type. These products have an pixel size of 12 × 12 µm and are available in the photosensitive area ranging from 24.576 (H) × 1.464 (V) mm^2 (2048 × 122 pixels) to 24.576 (H) × 6.072 (V) mm^2 (2048 × 506 pixels).

Features

- **Wide dynamic range**
- **Low readout noise: 4 e^- rms typ. [S10140/S10141 series (-01)]**
  30 e^- rms typ. (S13240/S13241 series)
- **High resolution: pixel size 12 × 12 µm**
- **Non-cooled type: S13240 series, S10140 series (-01)**
  One-stage TE-cooled type: S13241 series, S10141 series (-01)
- **Quantum efficiency: 90% or higher at peak**
- **Wide spectral response range**
- **MPP operation**
- **High UV sensitivity and stable characteristics under UV light irradiation**
- **Pin compatible with the S7030/S7031 series [S10140/S10141 series (-01)]**

Applications

- **Fluorescence spectrophotometry, ICP**
- **Industrial product inspection**
- **Semiconductor inspection**
- **DNA sequencer**
- **Low-light-level detection**
- **Raman spectroscopy**

Selection guide

Type no.	Cooling	Readout speed max. (MHz)	Total number of pixels (H) × (V)	Number of effective pixels (H) × (V)	Image size mm (H) × mm (V)
S13240-1107	Non-cooled	10	2068 × 128	2048 × 122	24.576 × 1.464
S13240-1108			2068 × 256	2048 × 250	24.576 × 3.000
S13240-1109			2068 × 512	2048 × 506	24.576 × 6.072
S13241-1107S	One-stage TE-cooled	10	2068 × 128	2048 × 122	24.576 × 1.464
S13241-1108S			2068 × 256	2048 × 250	24.576 × 3.000
S13241-1109S			2068 × 512	2048 × 506	24.576 × 6.072
S10140-1107-01	Non-cooled	0.5	2068 × 128	2048 × 122	24.576 × 1.464
S10140-1108-01			2068 × 256	2048 × 250	24.576 × 3.000
S10140-1109-01			2068 × 512	2048 × 506	24.576 × 6.072
S10141-1107S-01	One-stage TE-cooled	0.5	2068 × 128	2048 × 122	24.576 × 1.464
S10141-1108S-01			2068 × 256	2048 × 250	24.576 × 3.000
S10141-1109S-01			2068 × 512	2048 × 506	24.576 × 6.072

Note: S10142 series (-01) [Two-stage TE-cooled type] is available upon request (made-to-order products).

Structure

Parameter	S13240 series	S13241 series	S10140 series (-01)	S10141 series (-01)
Pixel size (H × V)	12 × 12 µm			
Vertical clock	2-phase			
Horizontal clock	2-phase			
Output circuit	Two-stage MOSFET source follower		One-stage MOSFET source follower	
Package	24-pin ceramic DIP (refer to dimensional outlines)			
Window material*1	Quartz glass*2	AR-coated sapphire*3	Quartz glass*2	AR-coated sapphire*3

*1: Temporary window type (ex. S13240-1107N) can also be provided.
*2: Resin sealing
*3: Hermetic sealing

Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Operating temperature*4		Topr	-50	-	+50	°C
Storage temperature		Tstg	-50	-	+70	°C
Output transistor drain voltage	S13240/S13241 series	V_{OD}	-0.5	-	+20	V
	S10140/S10141 series (-01)		-0.5	-	+25	
Reset drain voltage		V_{RD}	-0.5	-	+18	V
Output amplifier return voltage	S13240/S13241 series	Vret	-0.5	-	+18	V
Horizontal input source voltage		V_{ISH}	-0.5	-	+18	V
Vertical input gate voltage		V_{IG1V}, V_{IG2V}	-11	-	+15	V
Horizontal input gate voltage		V_{IG1H}, V_{IG2H}	-11	-	+15	V
Summing gate voltage		V_{SG}	-11	-	+15	V
Output gate voltage		V_{OG}	-11	-	+15	V
Reset gate voltage		V_{RG}	-11	-	+15	V
Transfer gate voltage		V_{TG}	-11	-	+15	V
Vertical shift register clock voltage		V_{P1V}, V_{P2V}	-11	-	+15	V
Horizontal shift register clock voltage		V_{P1H}, V_{P2H}	-11	-	+15	V
Soldering conditions*5		Tsol	260 °C, within 5 s, at least 2 mm away from lead roots			-
Maximum current of built-in TE-cooler*6		Imax	-	-	3.0	A
Maximum voltage of built-in TE-cooler		Vmax	-	-	3.6	V
Maximum temperature of heat radiation side		-	-	-	70	°C

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.
*4: Package temperature [S13240 series, S10140 series (-01)], chip temperature [S13241 series, S10141 series (-01)]
*5: Use a soldering iron.
*6: When the current value exceeds Imax, the heat absorption begins to decrease due to the Joule heat. This maximum current Imax is not the threshold for damaging the thermoelectric cooler. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.

Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	S13240/S13241 series			S10140/S10141 series (-01)			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Output transistor drain voltage			V_{OD}	14	16	18	20	22	24	V
Reset drain voltage			V_{RD}	15	16	17	14	15	16	V
Output gate voltage			V_{OG}	3	5	7	3	5	7	V
Substrate voltage			V_{SS}	-	0	-	-	0	-	V
Output amplifier return voltage*7			Vret	-	4	5				V
Test point	Input source		V_{ISH}	-	V_{RD}	-	-	V_{RD}	-	V
	Vertical input gate		V_{IG1V}, V_{IG2V}	-10	-9	-	-10	-9	-	
	Horizontal input gate		V_{IG1H}, V_{IG2H}	-10	-9	-	-10	-9	-	
Vertical shift register clock voltage		High	V_{P1VH}, V_{P2VH}	1	3	5	1	3	5	V
		Low	V_{P1VL}, V_{P2VL}	-10	-9	-8	-10	-9	-8	
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH}	5	7	9	5	7	9	V
		Low	V_{P1HL}, V_{P2HL}	-9	-7	-5	-9	-7	-5	
Summing gate voltage		High	V_{SGH}	5	7	9	5	7	9	V
		Low	V_{SGL}	-9	-7	-5	-9	-7	-5	
Reset gate voltage		High	V_{RGH}	8	9	10	8	9	10	V
		Low	V_{RGL}	-6	-5	-4	-6	-5	-4	
Transfer gate voltage		High	V_{TGH}	1	3	5	1	3	5	V
		Low	V_{TGL}	-10	-9	-8	-10	-9	-8	
External load resistance			R_L	2.0	2.2	2.4	20	22	24	kΩ

*7: Output amplifier return voltage is a positive voltage with respect to substrate voltage, but the current flows out from the sensor.

Electrical characteristics (Ta=25 °C)

Parameter		Symbol	S13240/S13241 series			S10140/S10141 series (-01)			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output signal frequency*8		fc	-	2.5	10	-	0.25	0.5	MHz
Vertical shift register capacitance	-1107 (-01)	C_{P1V}, C_{P2V}	-	1600	-	-	1600	-	pF
	-1108 (-01)		-	3200	-	-	3200	-	
	-1109 (-01)		-	6400	-	-	6400	-	
Horizontal shift register capacitance		C_{P1H}, C_{P2H}	-	150	-	-	150	-	pF
Summing gate capacitance		C_{SG}	-	30	-	-	30	-	pF
Reset gate capacitance		C_{RG}	-	30	-	-	30	-	pF
Transfer gate capacitance		C_{TG}	-	70	-	-	70	-	pF
Charge transfer efficiency*9		CTE	0.99995	0.99999	-	0.99995	0.99999	-	-
DC output level*8		Vout	10	11	12	16	17	18	V
Output impedance*8		Zo	-	0.2	-	-	5	-	kΩ
Power consumption*8 *10		P	-	100	-	-	16	-	mW

*8: The values depend on the load resistance (S13240/S13241 series: V_{OD}=16 V, R_L=2.2 kΩ, S10140/S10141 series (-01): V_{OD}=22 V, R_L=22 kΩ)
*9: Charge transfer efficiency per pixel, measured at half of the saturation output
*10: Power consumption of the on-chip amp plus load resistance

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

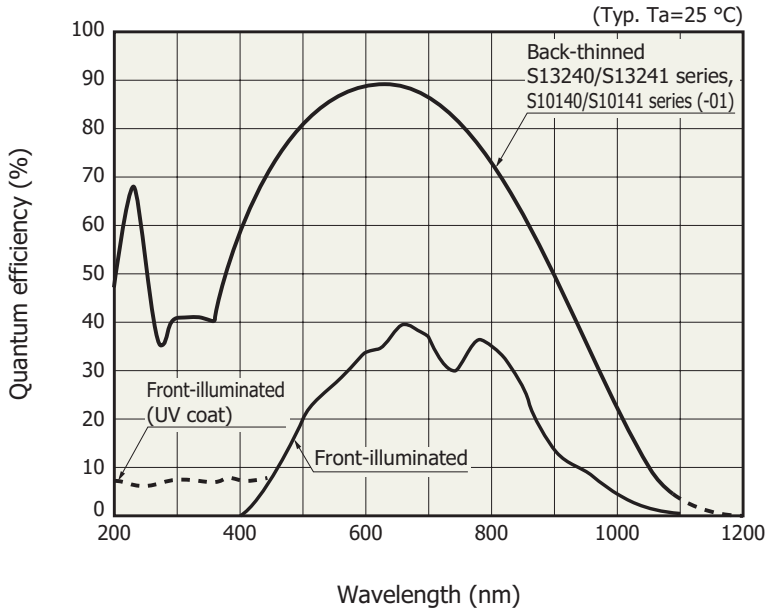
Parameter			Symbol	S13240/S13241 series			S10140/S10141 series (-01)			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Saturation output voltage			Vsat	-	Fw × Sv	-	-	Fw × Sv	-	V
Full well capacity	Vertical		Fw	60	70	-	60	70	-	ke⁻
	Horizontal			400	500	-	400	500	-	
	Summing			400	500	-	400	500	-	
CCD node sensitivity			Sv	4.5	5.5	6.5	4	5	6	μV/e⁻
Dark current*11	25 °C		DS	-	30	300	-	30	300	e⁻/pixel/s
MPP mode	0 °C			-	3	30	-	3	30	
Readout noise*12			Nr	-	30	45	-	4	18	e⁻ rms
Dynamic range*13	Line binning		DR	13333	16666	-	100000	125000	-	-
	Area scanning			2000	2333	-	15000	20000	-	-
Photoresponse nonuniformity*14			PRNU	-	±3	±10	-	±3	±10	%
Spectral response range			λ	-	200 to 1100	-	-	200 to 1100	-	nm
Blemish	Point defect*15	White spots	-	-	-	0	-	-	0	-
		Black spots		-	-	10	-	-	10	-
	Cluster defect*16			-	-	3	-	-	3	-
	Column defect*17			-	-	0	-	-	0	-

*11: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*12: Operating frequency 20 kHz, temperature -50 ºC [S10140/S10141 series (-01)]
Operating frequency 2.5 MHz, temperature 0 ºC (S13240/S13241 series)
*13: Dynamic range=Saturation charge/Readout noise
*14: Measured at one-half of the saturation output using LED light (peak emission wavelength: 470 nm)

$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100\ [\%]$$

*15: White spots
Pixels whose dark current is higher than 1 ke⁻ after one-second integration at a cooling temperature of 0 °C
Black spots
Pixels whose sensitivity is lower than one half of the average pixel output (measured with uniform light producing one-half of the saturation charge)
*16: 2 to 9 consecutive image defects
*17: 10 or more consecutive image defects

Spectral response (without window)*18



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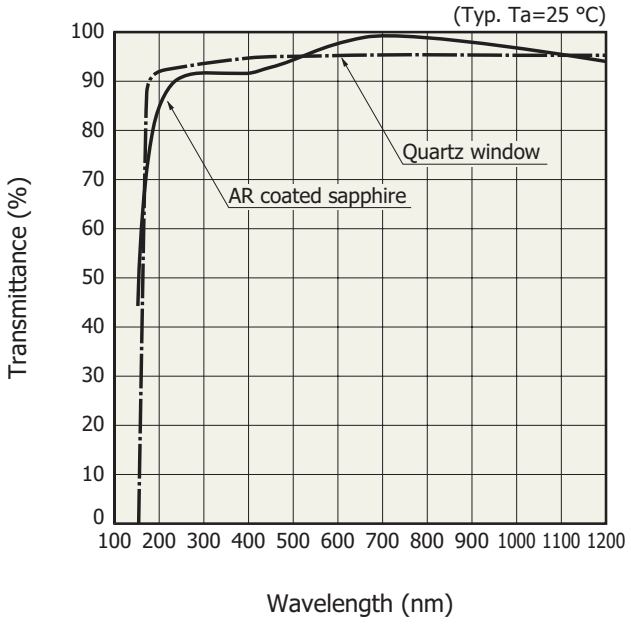
*18: Spectral response with quartz glass or AR-coated sapphire are decreased according to the spectral transmittance characteristics of window material.

Spectral transmittance characteristics



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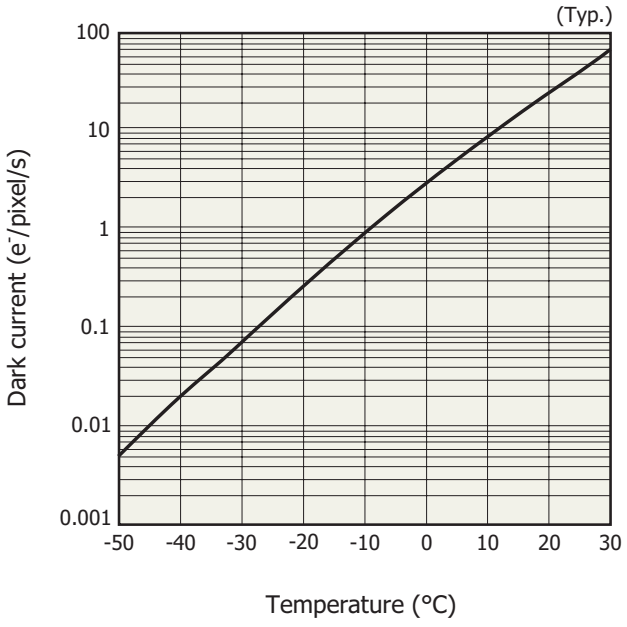
Dark current vs. temperature



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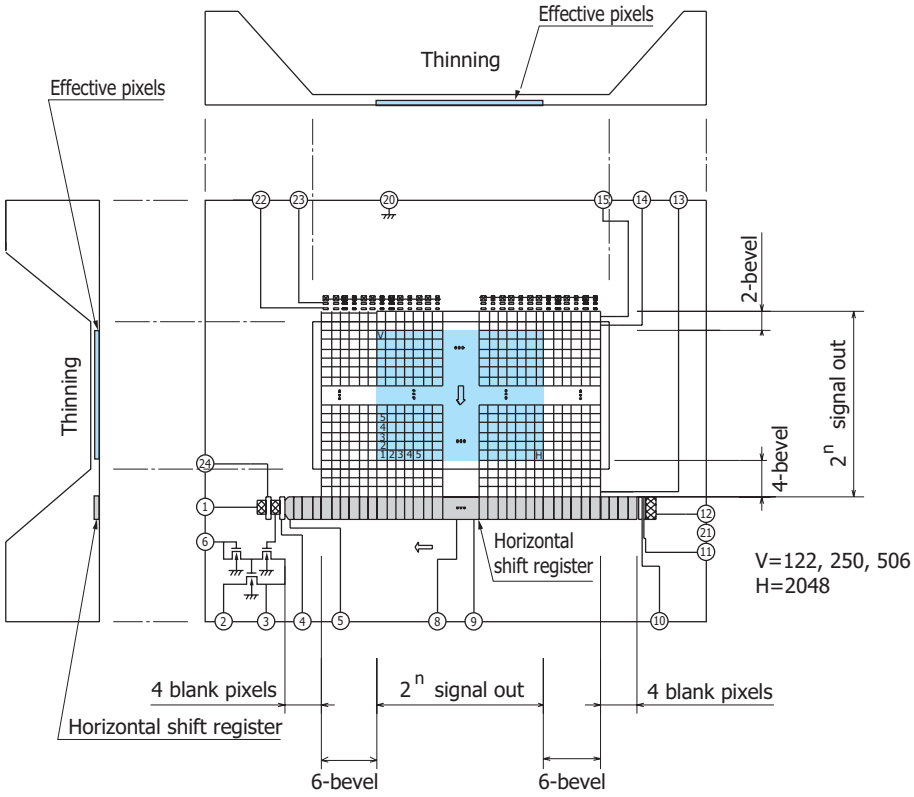
Device structure (schematic of CCD chip as viewed from top of dimensional outline)

S13240/S13241 series



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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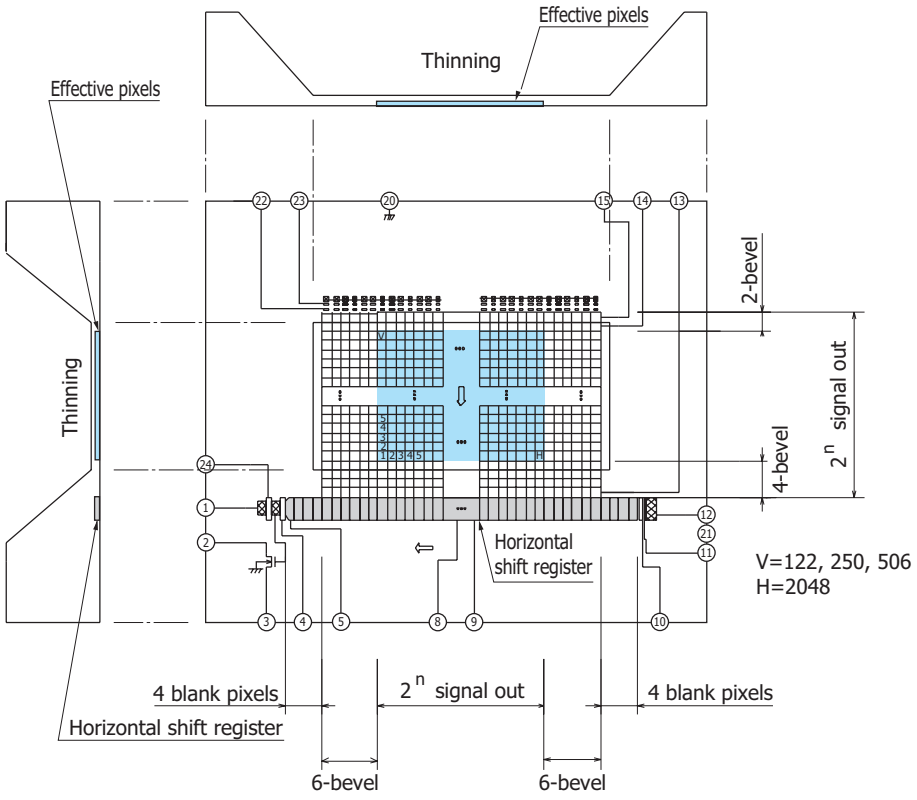
S10140/S10141 series (-01)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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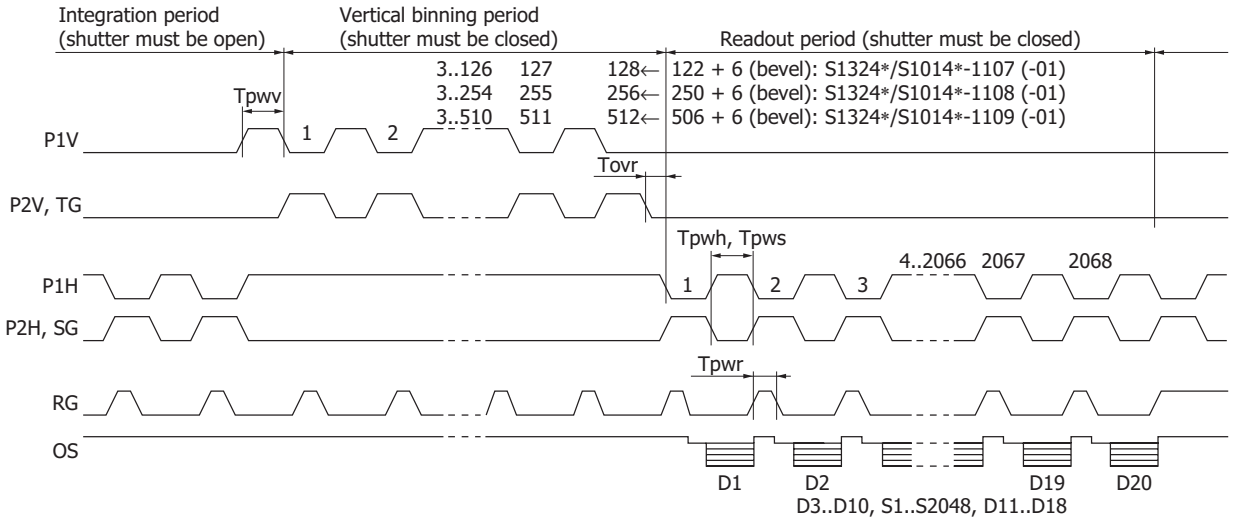
Timing chart

Line binning



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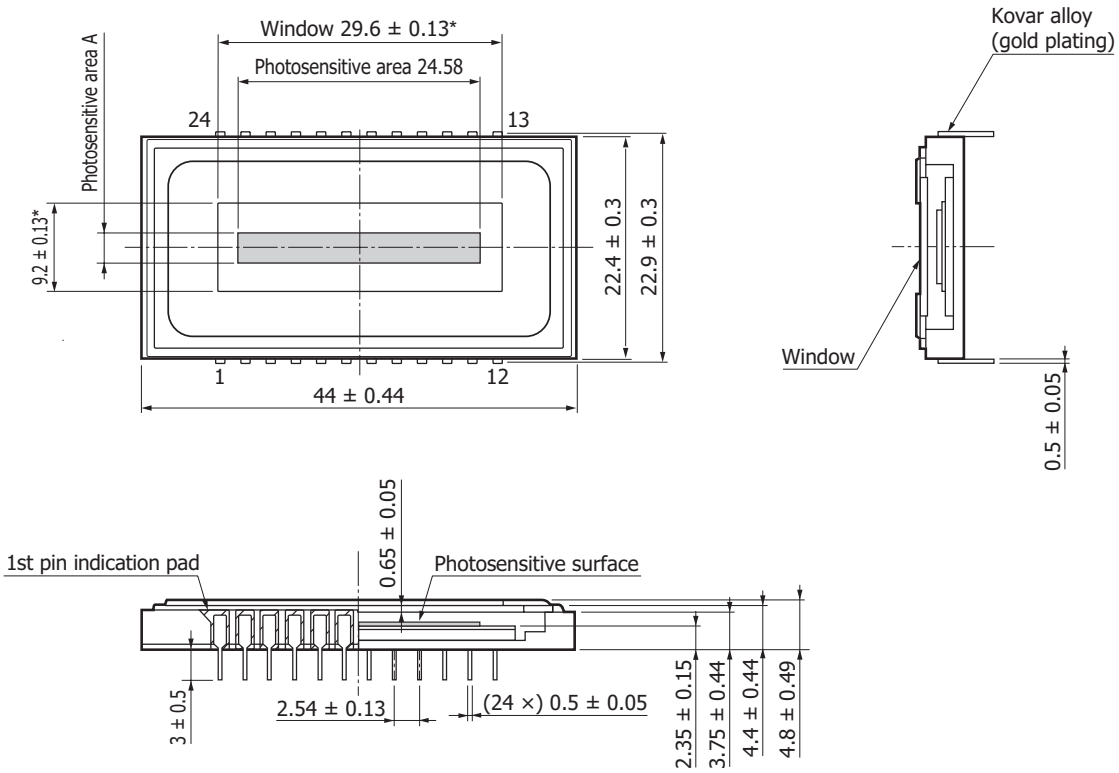
Parameter			Symbol	S13240/S13241 series			S10140/S10141 series (-01)			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
P1V, P2V, TG*19	Pulse width	-1107 (-01)	Tpwv	0.75	1	-	3	4	-	µs
		-1108 (-01)		1.5	2	-	6	8	-	
		-1109 (-01)		3	4	-	12	16	-	
	Rise and fall times		Tprv, Tpfv	20	-	-	20	-	-	ns
P1H, P2H*19	Pulse width		Tpwh	50	200	-	1000	2000	-	ns
	Rise and fall times		Tprh, Tpfh	10	-	-	10	-	-	ns
	Duty ratio		-	40	50	60	40	50	60	%
SG	Pulse width		Tpws	50	200	-	1000	2000	-	ns
	Rise and fall times		Tprs, Tpfs	10	-	-	10	-	-	ns
	Duty ratio		-	40	50	60	40	50	60	%
RG	Pulse width		Tpwr	10	40	-	100	1000	-	ns
	Rise and fall times		Tprr, Tpfr	5	-	-	5	-	-	ns
TG – P1H	Overlap time		Tovr	1	2	-	1	2	-	µs

*19: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)

S13240 series, S10140 series (-01)



S13240/S10140-1107 (-01): A=1.464
S13240/S10140-1108 (-01): A=3.000
S13240/S10140-1109 (-01): A=6.072

* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph is 28.6 × 8.2 mm.
weight: 11.9 g

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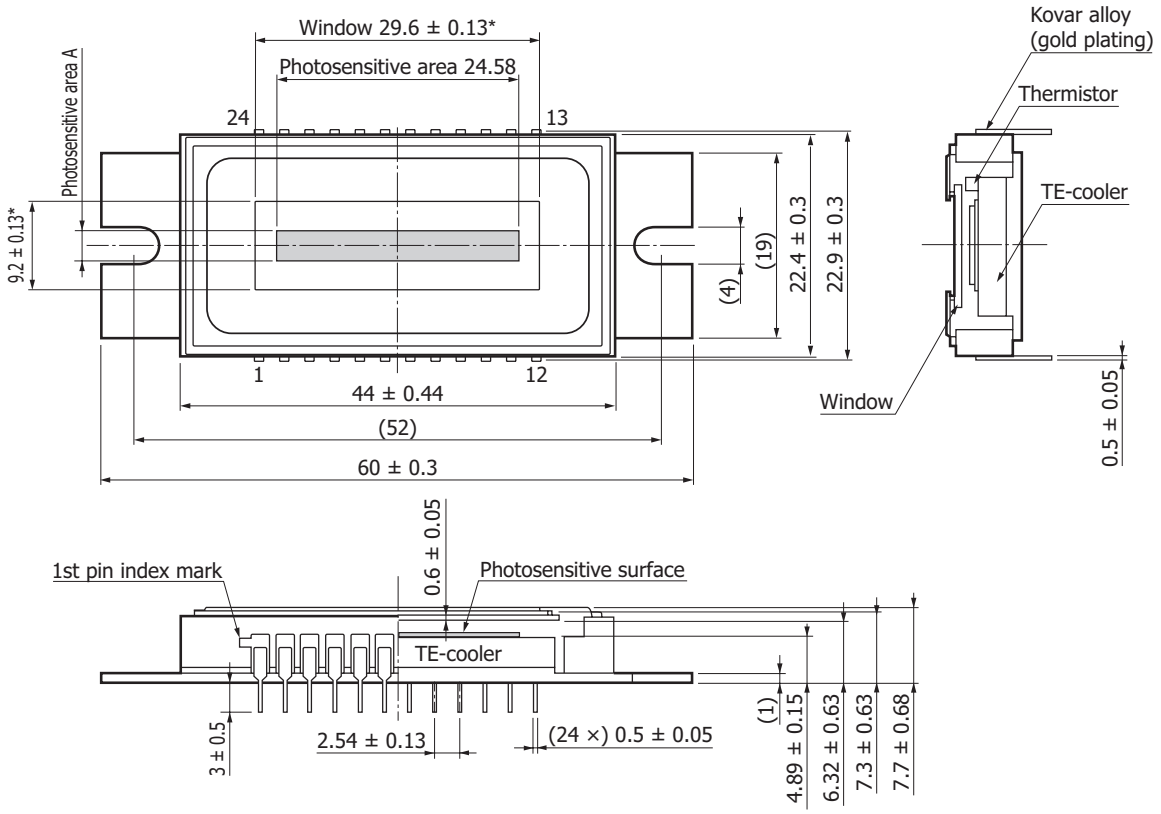
S13241 series, S10141 series (-01)



S13241/S10141-1107S (-01): A=1.464
S13241/S10141-1108S (-01): A=3.000
S13241/S10141-1109S (-01): A=6.072

* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics" graph is 27.6 × 7.2 mm.
Weight: 38.7 g

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Pin connections

Pin No.	S13240 series		S13241 series		Remark (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+16 V
2	OS	Output transistor source	OS	Output transistor source	RL=2.2 kΩ
3	OD	Output transistor drain	OD	Output transistor drain	+16 V
4	OG	Output gate	OG	Output gate	+5 V
5	SG	Summing gate	SG	Summing gate	Same timing as P2H
6	Vret	Output amplifier return	Vret	Output amplifier return	+4 V
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	-9 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	-9 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG*20	Transfer gate	TG*20	Transfer gate	Same timing as P2V
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler (-)	
19	-		P+	TE-cooler (+)	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	RD	Reset drain	RD	Reset drain	+16 V
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	-9 V
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	-9 V
24	RG	Reset gate	RG	Reset gate	

*20: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

Pin No.	S10140 series (-01)		S10141 series (-01)		Remark (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+15 V
2	OS	Output transistor source	OS	Output transistor source	RL=22 kΩ
3	OD	Output transistor drain	OD	Output transistor drain	+22 V
4	OG	Output gate	OG	Output gate	+5 V
5	SG	Summing gate	SG	Summing gate	Same timing as P2H
6	-		-		
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	-9 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	-9 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Connect to RD
13	TG*21	Transfer gate	TG*21	Transfer gate	Same timing as P2V
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler (-)	
19	-		P+	TE-cooler (+)	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	RD	Reset drain	RD	Reset drain	+15 V
22	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	-9 V
23	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	-9 V
24	RG	Reset gate	RG	Reset gate	

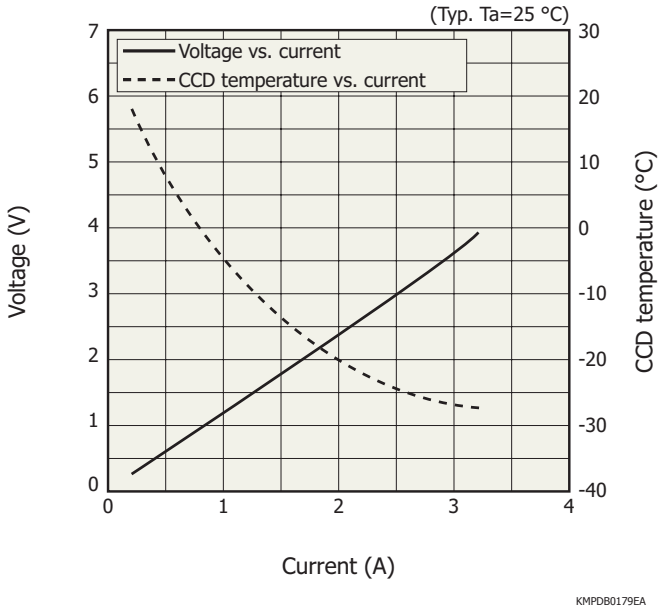
*21: Isolation gate between vertical register and horizontal register. In standard operation, TG should be applied the same pulse as P2V.

Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	S13241 series, S10141 series (-01)	Unit
Internal resistance	Rint	Ta=25 °C	1.2	Ω
Maximum heat absorption*22	Qmax		5.1	W

*22: This is a theoretical heat absorption level for correcting the temperature difference that occurs in the thermoelectric cooler when the maximum current is supplied.

S13241 series, S10141 series (-01)



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To make the cooling side -10 °C, the temperature on the heat radiation side must be 30 °C or less. As a guideline, use a heatsink whose thermal resistance is no more than 1 °C /W.

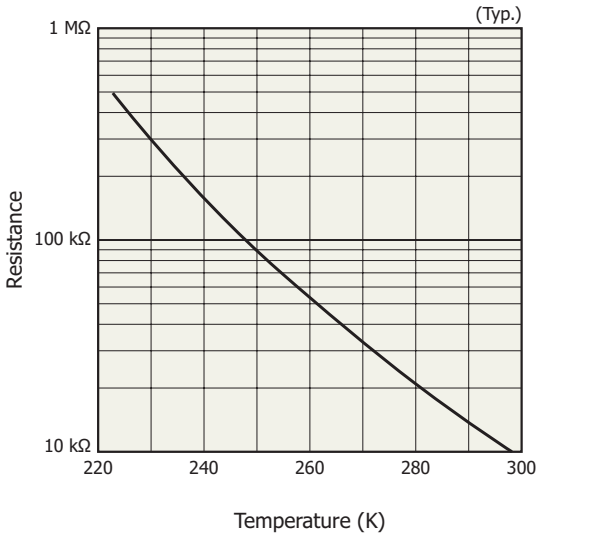
Specifications of built-in temperature sensor

A thermistor chip is built into the same package with a CCD chip and monitors the operating CCD chip temperature.
The relation between this thermistor's resistance and absolute temperature is express by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$

R_{T1}: resistance at absolute temperature T1 [K]
R_{T2}: resistance at absolute temperature T2 [K]
$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.
R_{298}=10 kΩ
$B_{298/323}$=3450 K



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Precautions (electrostatic countermeasures)

· Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
· Do not place the sensor directly on workbenches or floors that may become charged with static electricity.
· Connect a ground wire to workbenches or floors in order to discharge static electricity.
· Ground tools, such as tweezers and soldering irons, that are used to handle the sensor.

It is not always necessary to provide all the electrostatic countermeasures stated above. Implement these countermeasures according to the extent of deterioration or damage that may occur.

Temperature gradient rate for cooling or heating of element

When using an external cooler, set the temperature gradient rate for cooling or heating the element to 5 K/minute or less.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

■ Technical information
· FFT-CCD area image sensor/Technical information
· Image sensors/Terminology

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