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CCD linear image sensor

S14290

High-speed line rate

The S14290 is a back-thinned CCD linear image sensor that has achieved a high-speed line rate (30 kHz max.) with multiport readout (10 MHz max. per port).

Features

- **High-speed line rate: 30 kHz max.**

Applications

- **OCT (optical coherence tomography)**
- **Spectrophotometry**

Structure

Parameter	Specification
Image size (H × V)	24.576 × 0.500 mm
Pixel size (H × V)	24 × 500 µm
Number of total pixels (H × V)	1056 × 1
Number of effective pixels (H × V)	1024 × 1
Horizontal clock phase	2 phases
Output circuit	Two-stage MOSFET source follower
Package	54-pin ceramic DIP (refer to dimensional outline)
Window*2	Borosilicate glass*1
Cooling	Non-cooled

*1: Resin sealing
*2: Window-less type (ex. S14290N) is available upon request. (Temporary window is fixed by tape to protect the CCD chip.)

Absolute maximum ratings (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Operating temperature*2 *3		Topr	-50	-	+50	°C
Storage temperature		Tstg	-50	-	+70	°C
Output transistor drain voltage		VOD	-0.5	-	+25	V
Reset drain voltage		VRD	-0.5	-	+18	V
Output amplifier return voltage		Vret	-0.5	-	+18	V
All reset drain voltage		VARD	-0.5	-	+18	V
Horizontal input source voltage		VISH	-0.5	-	+18	V
All reset gate voltage		VARG	-10	-	+15	V
Storage gate voltage		VSTG	-10	-	+15	V
Horizontal input gate voltage		VIG1H, VIG2H	-10	-	+15	V
Summing gate voltage		VSG	-10	-	+15	V
Output gate voltage		VOG	-10	-	+15	V
Reset gate voltage		VRG	-10	-	+15	V
Transfer gate voltage		VTG	-10	-	+15	V
Resistive gate voltage	High	VREGH	-10	-	+15	V
	Low	VREGL				
Horizontal shift register clock voltage		VP1H, VP2H	-10	-	+15	V
Soldering conditions*4		Tsol	260 °C, within 5 s, at least 2 mm away from lead roots			-

*2: Package temperature
*3: The sensor temperature may increase due to heating in high-speed operation. We recommend taking measures to dissipate heat as needed. For more details, refer to the technical information "Resistive gate type CCD linear image sensors with electronic shutter".
*4: Use a soldering iron.
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		VOD	12	15	18	V
Reset drain voltage		VRD	14	15	16	V
Output amplifier return voltage*5		Vret	-	1	2	V
All reset drain voltage		VARD	11	12	13	V
Test point	Horizontal input source	VISH	-	VRD	-	V
	Horizontal input gate	VIG1H, VIG2H	-9	-8	-	
All reset gate voltage		VARGL	-6.5	-6	-5.5	V
Storage gate voltage*6		VSTG1	-1	0	0	V
		VSTG2	-1	0	1	V
Summing gate voltage	High	VSGH	5	6	7	V
	Low	VSGL	-6	-5	-4	
Output gate voltage		VOG	4.5	5	5.5	V
Reset gate voltage	High	VRGH	7	8	9	V
	Low	VRGL	-6	-5	-4	
Transfer gate voltage	High	VTGH	8	9	10	V
	Low	VTGL	-8	-7	-6	
Resistive gate high voltage		VREGH	-4	-3	-2	V
Resistive gate low voltage		VREGL	-	VREGH - 2.5	-	V
Horizontal shift register clock voltage	High	VP1HH, VP2HH	5	6	7	V
	Low	VP1HL, VP2HL	-6	-5	-4	
Substrate voltage		VSS	-	0	-	V
External load resistance		RL	2.0	2.2	2.4	kΩ

*5: Output amplifier return voltage is a positive voltage with respect to Substrate voltage, but the current flows in the direction of flow out of the sensor.
*6: Set VSTG1 lower than VSTG2.

Electrical characteristics [Ta=25 °C, operation conditions: Typ. (P.2)]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	5	10	MHz
Line rate	LR	-	10	30	kHz
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	200	-	pF
All reset gate capacitance	C_{ARG}	-	300	-	pF
Resistive gate capacitance	C_{REG}	-	1000	-	pF
Summing gate capacitance	C_{SG}	-	30	-	pF
Reset gate capacitance	C_{RG}	-	30	-	pF
Transfer gate capacitance	C_{TG}	-	300	-	pF
Charge transfer efficiency*7	CTE	0.99995	0.99999	-	-
DC output level	Vout	9	10	11	V
Output impedance	Zo	-	300	-	Ω
Output amplifier return current	Iret	-	0.4	-	mA
Power consumption	P_{AMP}*8	-	75	-	mW
	P_{REG}*9	0.6	3.1	6.3	
Resistive gate resistance*10	R_{REG}	0.5	1.5	5	kΩ

*7: Charge transfer efficiency per pixel of CCD shift register, measured at half of the full well capacity
*8: Power consumption of the on-chip amplifier plus load resistance
*9: Power consumption at REG
*10: Resistance value between REGH and REGL

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted, operating condition: Typ.)

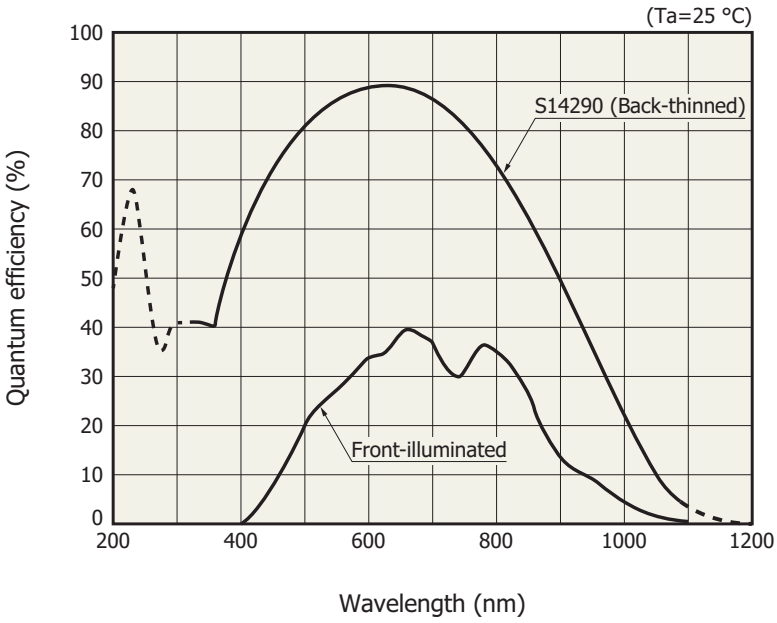
Parameter	Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage	Vsat	-	Fw × CE	-	V
Full well capacity	Fw	400	500	-	ke^-
Conversion efficiency	CE	4	5	6	$\mu V/e^-$
Dark current (Non-MPP mode)*11	DS	-	120	600	ke^-/pixel/s
		-	80	400	pA/cm²
Readout noise*12	Nread	-	100	150	e^- rms
Dynamic range*13	Drange	2600	5000	-	-
Spectral response range	λ	-	320 to 1100	-	nm
Photoresponse nonuniformity*14 *15	PRNU	-	±3	±10	%
Image lag*14 *16	L	-	10	20	%

*11: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*12: Signal outoput frequency=10 MHz
*13: Dynamic range=Full well capacity/Readout noise
*14: Measured at one-half of the saturation output (full well capacity), using LED light

*15: Photoresponse nonuniformity = $\frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$ [%]

*16: The ratio of remaining signal after the image sensor is illuminated with one shot of pulsed light that produces one-half of the saturation output. For more details refer to our technical information on "Resistive gate type CCD linear image sensors with electronic shutter."

Spectral response (typical example, without window)*17



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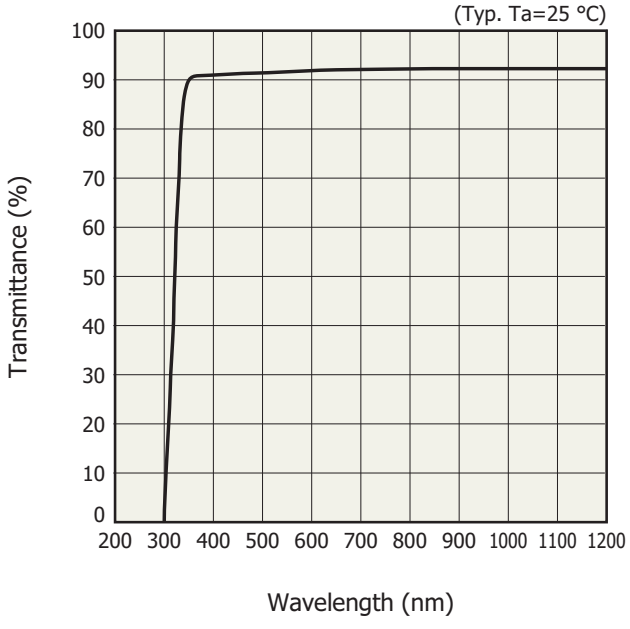
*17: Spectral response with borosilicate glass is decreased according to the spectral transmittance characteristics of window material.

Spectral transmittance characteristics of window material



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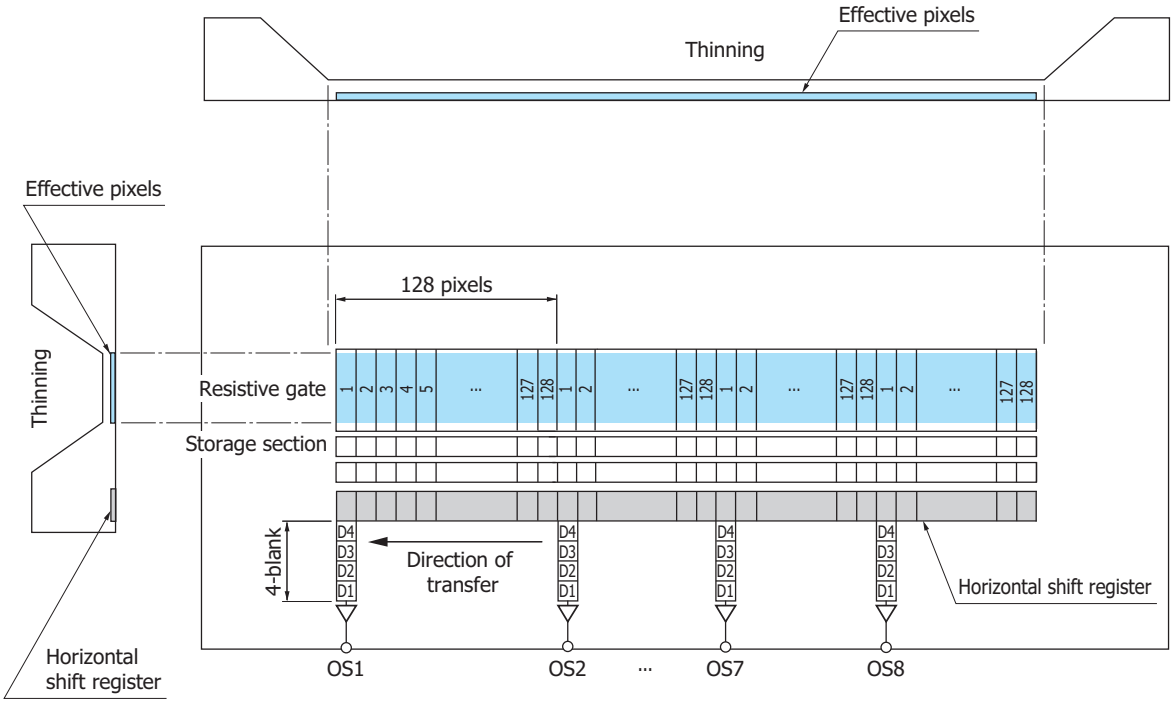
Device structure (conceptual drawing of top view in dimensional outline)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

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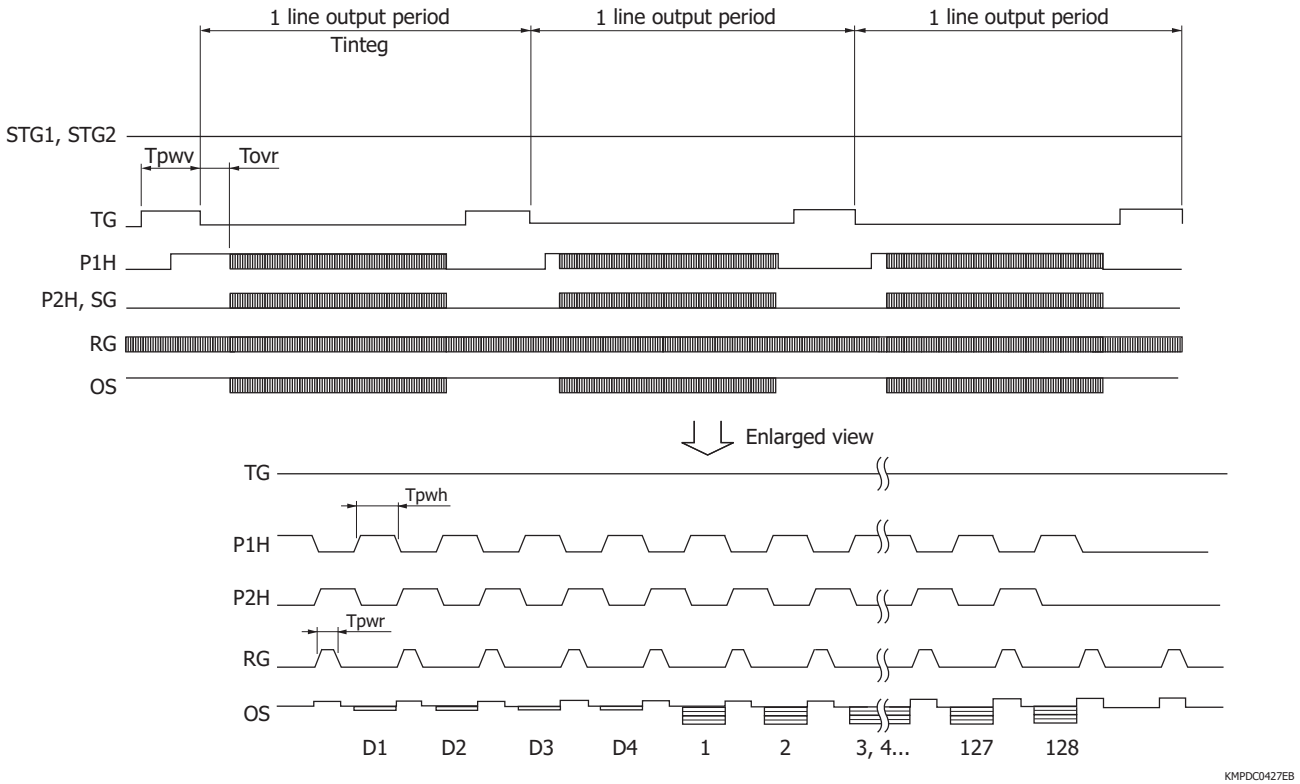
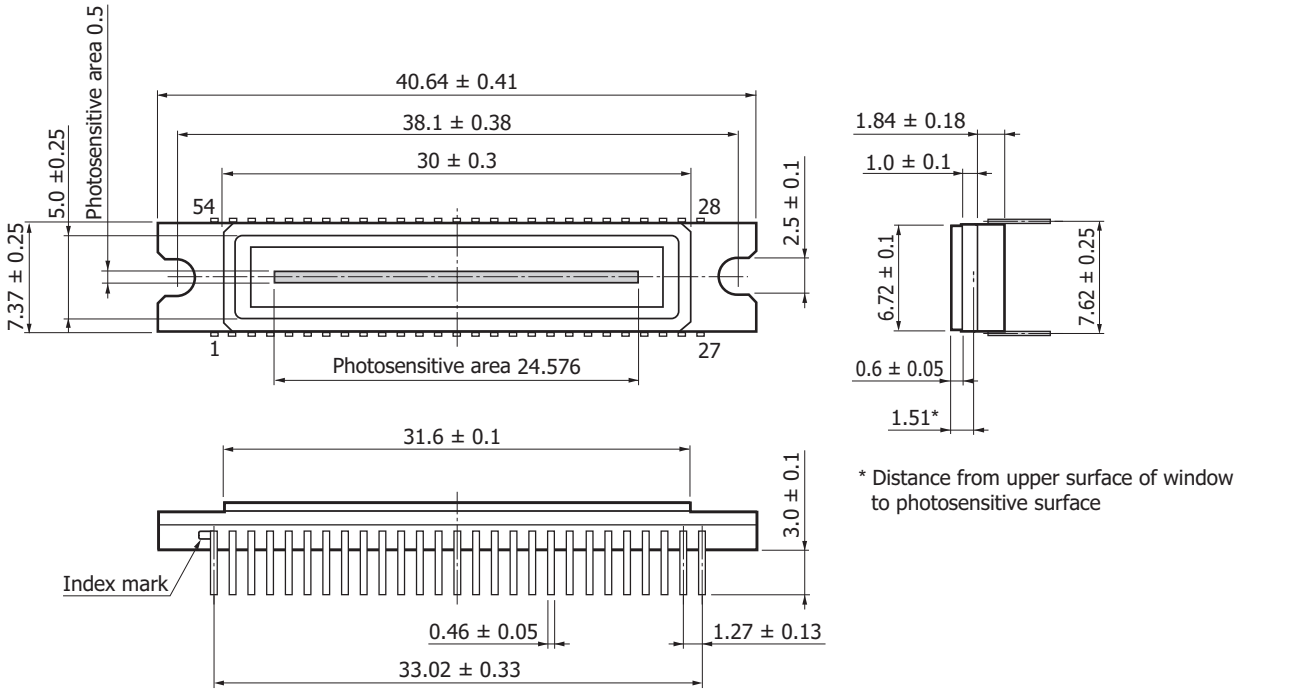
Timing chart



Parameter		Symbol	Min.	Typ.	Max.	Unit
TG	Pulse width	Tpwv	0.6	1.2	-	µs
	Rise and fall times	Tprv, Tpfv	20	-	-	ns
P1H, P2H*18	Pulse width	Tpwh	50	100	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	40	50	60	%
SG	Pulse width	Tpws	50	100	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	40	50	60	%
RG	Pulse width	Tpwr	5	15	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG - P1H	Overlap time	Tovr	200	400	-	ns
Integration time		Tinteg	33	66	-	µs

*18: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)



* Distance from upper surface of window to photosensitive surface

Weight: 3.5 g
Window refractive index: 1.52
AR coat: none

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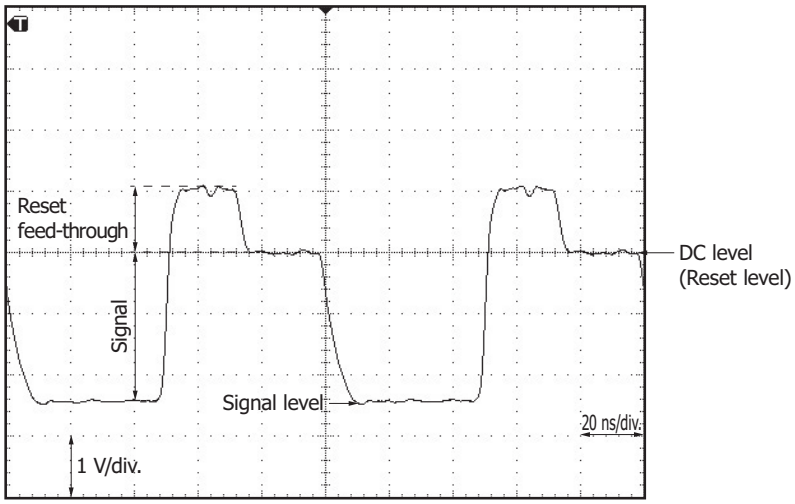
Pin connections

Pin no.	Symbol	Function	Remark (standard operation)
1	Vret	Output amplifier return	+1 V
2	OG	Output gate	+5 V
3	RD	Reset drain	+15 V
4	Vret	Output amplifier return	+1 V
5	OS1	Output transistor source 1	RL=2.2 kΩ
6	OD1	Output transistor drain 1	+15 V
7	OS2	Output transistor source 2	RL=2.2 kΩ
8	OD2	Output transistor drain 2	+15 V
9	Vret	Output amplifier return	+1 V
10	OS3	Output transistor source 3	RL=2.2 kΩ
11	OD3	Output transistor drain 3	+15 V
12	OS4	Output transistor source 4	RL=2.2 kΩ
13	OD4	Output transistor drain 4	+15 V
14	Vret	Output amplifier return	+1 V
15	OS5	Output transistor source 5	RL=2.2 kΩ
16	OD5	Output transistor drain 5	+15 V
17	OS6	Output transistor source 6	RL=2.2 kΩ
18	OD6	Output transistor drain 6	+15 V
19	Vret	Output amplifier return	+1 V
20	OS7	Output transistor source 7	RL=2.2 kΩ
21	OD7	Output transistor drain 7	+15 V
22	OS8	Output transistor source 8	RL=2.2 kΩ
23	OD8	Output transistor drain 8	+15 V
24	Vret	Output amplifier return	+1 V
25	IGH	Test point (horizontal input gate)	-8 V
26	ISH	Test point (horizontal input source)	Connect to RD
27	Vret	Output amplifier return	+1 V
28	SS	Substrate	GND
29	TG	Transfer gate	
30	STG2	Storage gate 2	0 V
31	REGH	Resistive gate (High)	-3 V
32	STG1	Storage gate 1	0 V
33	SS	Substrate	GND
34	ARD	All reset drain	+12 V
35	ARG	All reset gate	
36	REGL	Resistive gate (Low)	-5.5 V
37	SS	Substrate	GND
38	SG	Summing gate	
39	SS	Substrate	GND
40	P1H	CCD horizontal shift register clock-1	
41	SS	Substrate	GND
42	P2H	CCD horizontal shift register clock-2	
43	SS	Substrate	GND
44	RG	Reset gate	
45	SS	Substrate	GND
46	REGL	Resistive gate (Low)	-5.5 V
47	ARG	All reset gate	
48	ARD	All reset drain	+12 V
49	SS	Substrate	GND
50	STG1	Storage gate 1	0 V
51	REGH	Resistive gate (High)	-3 V
52	STG2	Storage gate 2	0 V
53	TG	Transfer gate	
54	SS	Substrate	GND

OS output waveform example (fc=10 MHz, RL=2.2 kΩ, VOD=+15 V)



Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

■ Technical information
· Resistive gate type CCD linear image sensors with electronic shutter

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