

CCD image sensors



S16011 series

Enhanced near infrared sensitivity, Constant element temperature control

The S16011 series is a family of back-thinned FFT (full frame transfer)-CCD image sensors for photometric applications that offer improved sensitivity in the near infrared region at wavelengths longer than 800 nm. In addition to having high infrared sensitivity, the S16011 series can be used as an image sensor with a long photosensitive area in the direction of the sensor height by binning operation, making it suitable for detectors in Raman spectroscopy. Binning operation also ensures even higher S/N and signal processing speed compared to methods that use an external circuit to add signals digitally. In addition, a TE-cooler is built into the package to keep the element temperature constant (approx. 5 °C) during operation. The S16011 series has a pixel size of 14 × 14 μm and is available in two image areas of 14.336 (H) × 0.896 (V) mm (1024 × 64 pixels) and 28.672 (H) × 0.896 (V) mm (2048 × 64 pixels). The S16011 series is pin compatible with the S11850-1106, and so operates under the same drive conditions.

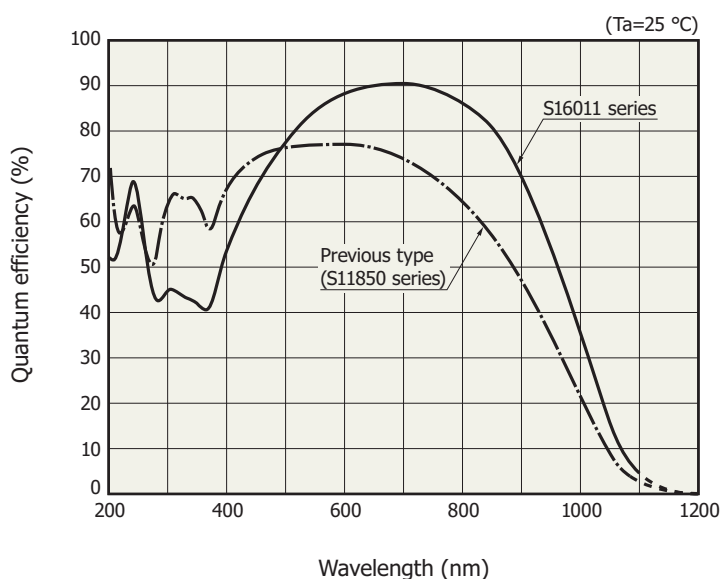
Features

- NIR high sensitivity: QE=36% (λ=1000 nm)
- One-stage TE-cooled type (element temperature: approx. 5 °C)
- High CCD node sensitivity: 6.5 μV/e⁻
- High full well capacity, wide dynamic range (with anti-blooming function)
- Pixel size: 14 × 14 μm
- MPP operation

Applications

- Raman spectrometers, etc.

Spectral response (without window, typical example)*1



KMPDB0596EA

*1: Spectral response with quartz glass is decreased according to the spectral transmittance characteristic of window material.

▣ Selection guide

| Type no. | Total number of pixels | Number of effective pixels | Image size [mm (H) × mm (V)] | Readout speed max. (MHz) | Suitable driver circuit |
|-------------|------------------------|----------------------------|---------------------------------|--------------------------------|-------------------------|
| S16011-1006 | 1044 × 70 | 1024 × 64 | 14.336 × 0.896 | 0.5 | C11860 |
| S16011-1106 | 2068 × 70 | 2048 × 64 | 28.672 × 0.896 | | |

▣ Structure

| Parameter | S16011-1006 | S16011-1106 | Unit |
|----------------------------|---|----------------|------|
| Image size (H × V) | 14.336 × 0.896 | 28.672 × 0.896 | mm |
| Pixel size (H × V) | 14 × 14 | | μm |
| Number of total pixels | 1044 × 70 | 2068 × 70 | - |
| Number of effective pixels | 1024 × 64 | 2048 × 64 | - |
| Vertical clock phase | 2-phase | | - |
| Horizontal clock phase | 4-phase | | - |
| Output circuit | One-stage MOSFET source follower | | - |
| Package | 28-pin ceramic DIP (refer to dimensional outline) | | - |
| Window | Quartz glass*2 | | - |

*2: Hermetic sealing

▣ Absolute maximum ratings (Ta = 25 °C, unless otherwise noted)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|--------------------------|-----------------|------|------|------|------|
| Operating temperature*3 | Topr | | -50 | - | +50 | °C |
| Storage temperature | Tstg | | -50 | - | +70 | °C |
| Output transistor drain voltage | VOD | | -0.5 | - | +30 | V |
| Reset drain voltage | VRD | | -0.5 | - | +18 | V |
| Overflow drain voltage | VOFD | | -0.5 | - | +18 | V |
| Vertical input source voltage | VISV | | -0.5 | - | +18 | V |
| Horizontal input source voltage | VISH | | -0.5 | - | +18 | V |
| Overflow gate voltage | VOFG | | -10 | - | +15 | V |
| Vertical input gate voltage | VIG1V, VIG2V | | -10 | - | +15 | V |
| Horizontal input gate voltage | VIG1H, VIG2H | | -10 | - | +15 | V |
| Summing gate voltage | VSG | | -10 | - | +15 | V |
| Output gate voltage | VOG | | -10 | - | +15 | V |
| Reset gate voltage | VRG | | -10 | - | +15 | V |
| Transfer gate voltage | VTG | | -10 | - | +15 | V |
| Vertical shift register clock voltage | VP1V, VP2V | | -10 | - | +15 | V |
| Horizontal shift register clock voltage | VP1H, VP2H VP3H, VP4H | | -10 | - | +15 | V |
| TE-cooler maximum current*4 *5 | Imax | Tc*6=Th*7=25 °C | - | 1.8 | - | A |
| TE-cooler maximum voltage | Vmax | Tc*6=Th*7=25 °C | - | 3.5 | - | V |
| Thermistor power dissipation | Pd_th | | - | - | 100 | mW |

*3: Chip temperature

*4: If the current greater than this value flows into the thermoelectric cooler, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not the damage threshold value. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60% of this maximum current.

*5: To ensure stable temperature control, ΔT (temperature difference between Th and Tc) should be less than 30 °C. If ΔT exceeds 30 °C, product characteristics may deteriorate. For example, the dark current uniformity may degrade.

*6: Temperature of the cooling side of thermoelectric cooler

*7: Temperature of the heat radiating side of thermoelectric cooler

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

▣ Operating conditions (MPP mode, Ta=25 °C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | |
|---|-----------------------|----------------------------|------|------|------|---|
| Output transistor drain voltage | VOD | 23 | 24 | 25 | V | |
| Reset drain voltage | VRD | 11 | 12 | 13 | V | |
| Overflow drain voltage | VOFD | 11 | 12 | 13 | V | |
| Test point | Input source | VISV, VISH | - | VRD | - | V |
| | Vertical input gate | VIG1V, VIG2V | -9 | -8 | - | V |
| | Horizontal input gate | VIG1H, VIG2H | -9 | -8 | - | V |
| Overflow gate voltage | VOFG | 0 | 12 | 13 | V | |
| Summing gate voltage | High | VSGH | 4 | 6 | 8 | V |
| | Low | VSGL | -6 | -5 | -4 | |
| Output gate voltage | VOG | 4 | 5 | 6 | V | |
| Reset gate voltage | High | VRGH | 4 | 6 | 8 | V |
| | Low | VRGL | -6 | -5 | -4 | |
| Transfer gate voltage | High | VTGH | 4 | 6 | 8 | V |
| | Low | VTGL | -9 | -8 | -7 | |
| Vertical shift register clock voltage | High | VP1VH, VP2VH | 4 | 6 | 8 | V |
| | Low | VP1VL, VP2VL | -9 | -8 | -7 | |
| Horizontal shift register clock voltage | High | VP1HH, VP2HH, VP3HH, VP4HH | 4 | 6 | 8 | V |
| | Low | VP1HL, VP2HL, VP3HL, VP4HL | -6 | -5 | -4 | |
| Substrate voltage | VSS | - | 0 | - | V | |
| External load resistance | RL | 90 | 100 | 110 | kΩ | |

▣ Electrical characteristics (Ta=25 °C, operating conditions: Typ.)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | |
|---------------------------------------|--------|------------------------|---------|------|------|----|
| Signal output frequency*8 | fc | - | 0.25 | 0.5 | MHz | |
| Vertical shift register capacitance | -1006 | CP1V, CP2V | - | 600 | - | pF |
| | -1106 | | | 1200 | | |
| Horizontal shift register capacitance | -1006 | CP1H, CP2H, CP3H, CP4H | - | 80 | - | pF |
| | -1106 | | | 160 | | |
| Summing gate capacitance | CSG | - | 10 | - | pF | |
| Reset gate capacitance | CRG | - | 10 | - | pF | |
| Transfer gate capacitance | -1006 | CTG | - | 30 | - | pF |
| | -1106 | | | 60 | | |
| Charge transfer efficiency*9 | CTE | 0.99995 | 0.99999 | - | - | |
| DC output level*8 | Vout | 17 | 18 | 19 | V | |
| Output impedance*8 | Zo | - | 10 | - | kΩ | |
| Power consumption*8 *10 | P | - | 4 | - | mW | |

*8: The values depend on the load resistance. (VOD=24 V, RL=100 kΩ)

*9: Charge transfer efficiency per pixel, measured at half of the full well capacity

*10: Power consumption of the on-chip amplifier plus load resistance

Electrical and optical characteristics (Ta=25 °C, operating conditions: Typ., unless otherwise noted)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|------------|-------|-------------|------|-------------------------|
| Saturation output voltage | Vsat | - | Fw × CE | - | V |
| Full well capacity | Vertical | 50 | 60 | - | ke ⁻ |
| | Horizontal | 250 | 300 | - | |
| Conversion efficiency*11 | CE | 5.5 | 6.5 | 7.5 | μV/e ⁻ |
| Dark current*12 | DS | - | 50 | 500 | e ⁻ /pixel/s |
| Readout noise*13 | Nread | - | 6 | 15 | e ⁻ rms |
| Dynamic range*14 Line binning | Drange | 41700 | 50000 | - | - |
| Spectral response range | λ | - | 200 to 1100 | - | nm |
| Photoresponse nonuniformity*15 | PRNU | - | ±3 | ±10 | % |

*11: The values depend on the load resistance (V_{OD}=24 V, R_L=100 kΩ).

*12: Dark current is reduced to half for every 5 to 7 °C decrease in temperature.

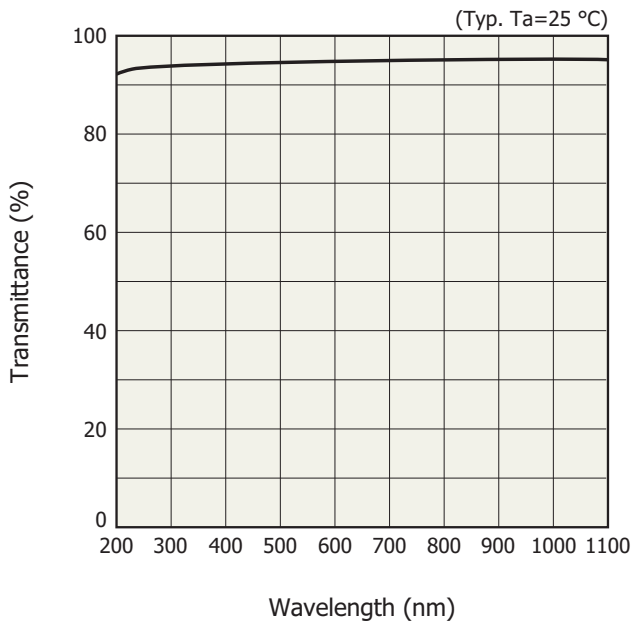
*13: Chip temperature: -40 °C, f_c=20 kHz

*14: Dynamic range = Full well capacity / Readout noise

*15: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 450 nm)

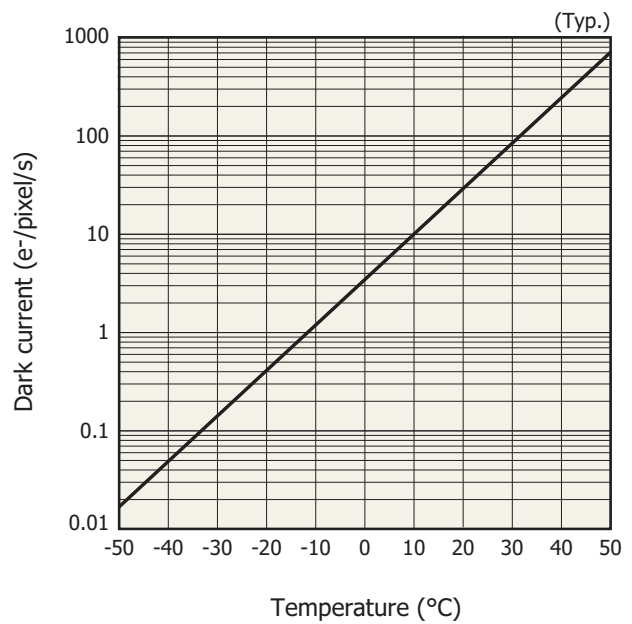
$$\text{Photoresponse nonuniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 [\%]$$

Spectral transmittance characteristics of window material



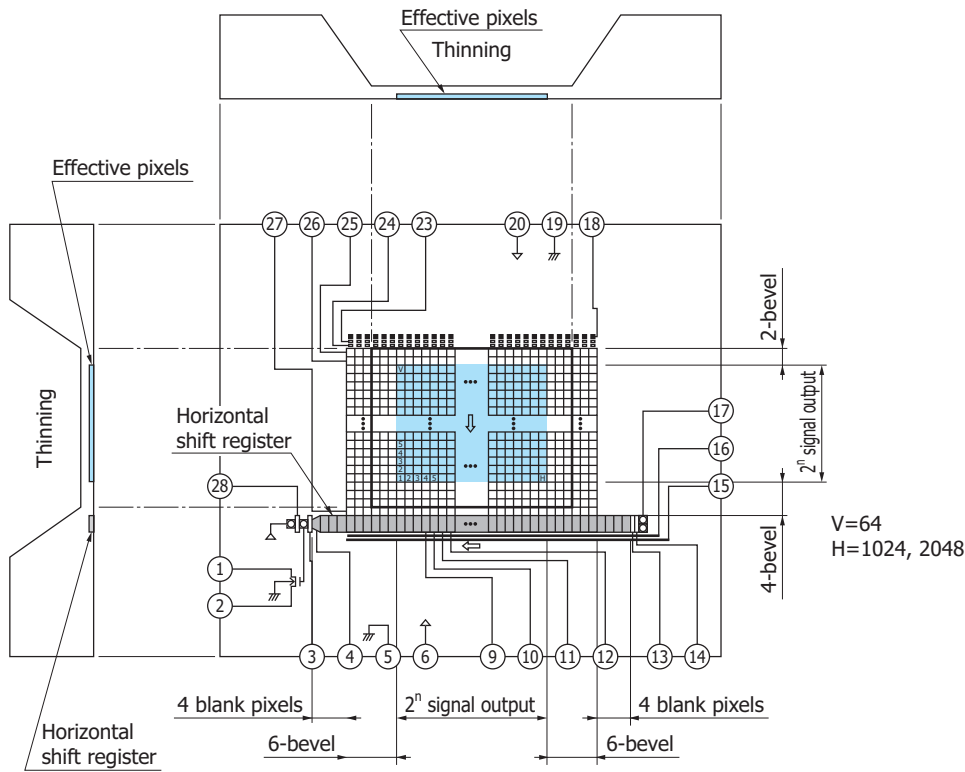
KMPDB0303EB

Dark current vs. temperature



KMPDB0304EB

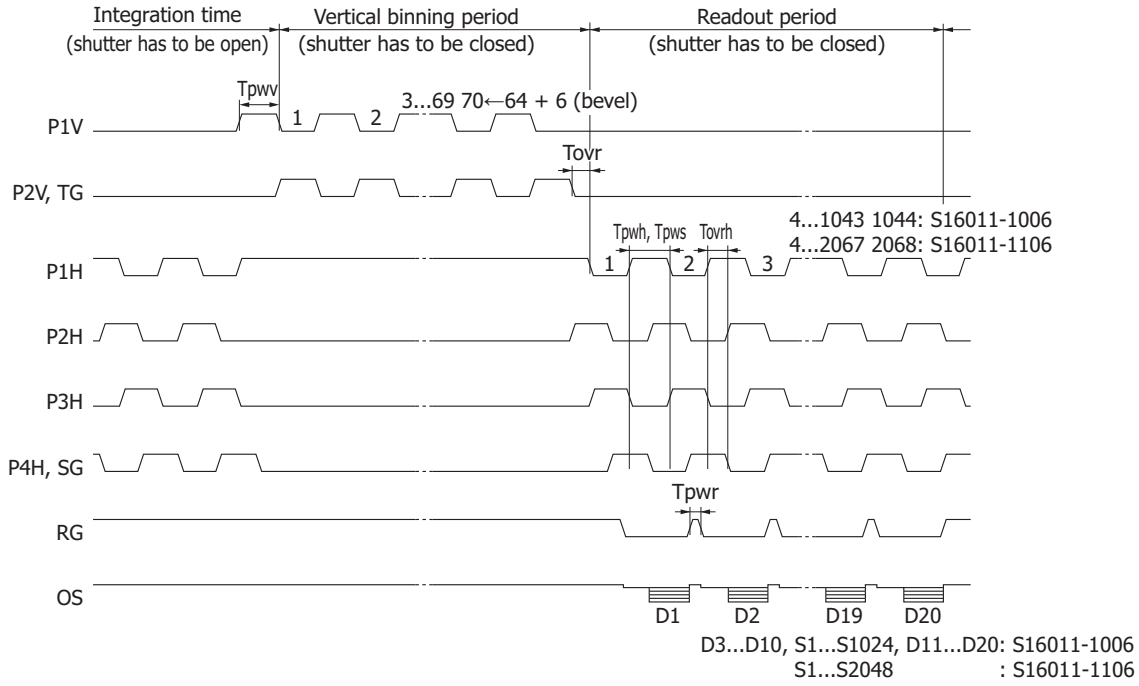
Device structure (schematic of CCD chip as viewed from top of dimensional outline)



Note: When viewed from the direction of the incident light, the horizontal shift register is covered with a thick silicon layer (dead layer). However, long-wavelength light passes through the silicon dead layer and may possibly be detected by the horizontal shift register. To prevent this, provide light shield on that area as needed.

KMPC00596EB

Timing chart (line binning)

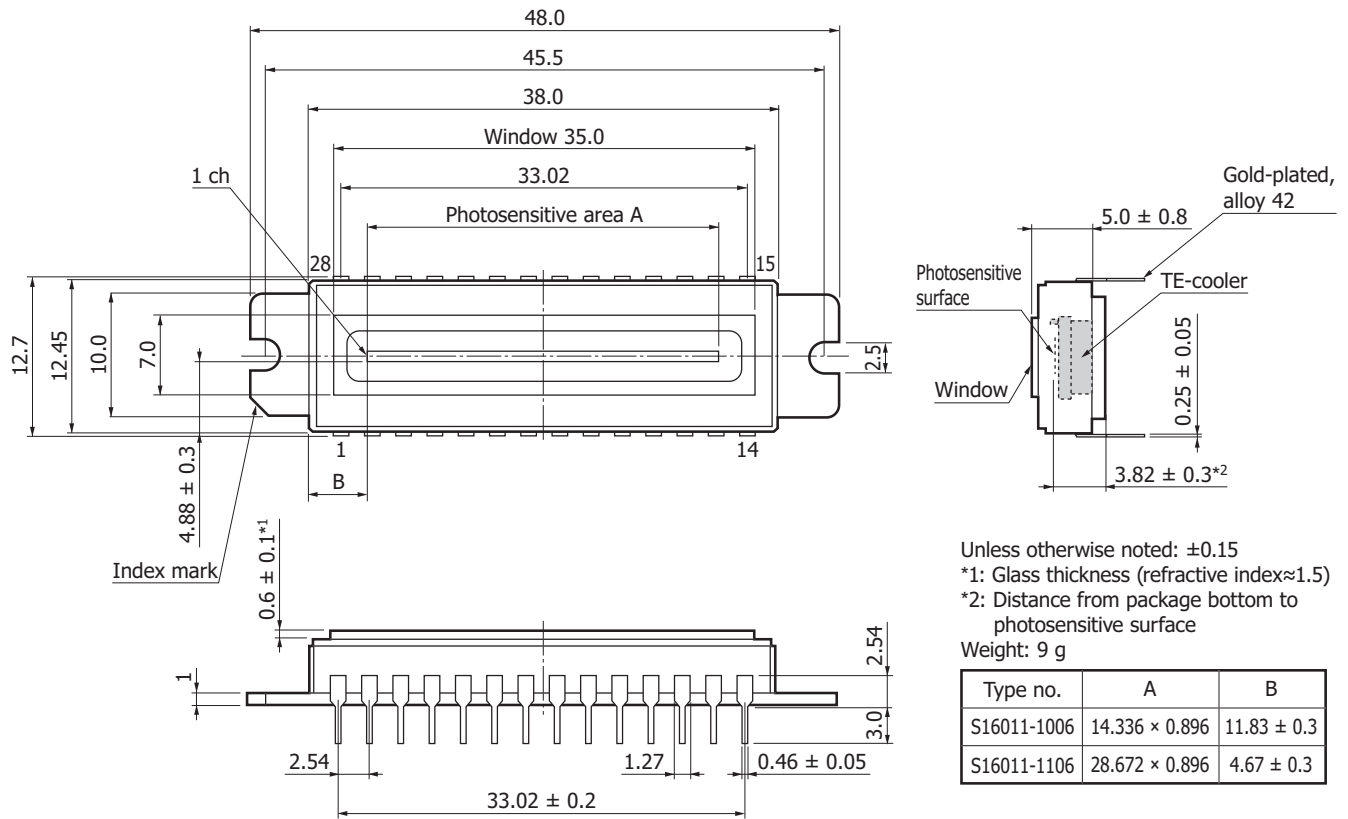


KMPDC0847EA

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|--------------------|------------------------|-------------|------|------|------|------|
| P1V, P2V, TG | Pulse width*16 | Tpww | 6 | 8 | - | µs |
| | Rise and fall times*16 | Tprv, Tpfv | 20 | - | - | ns |
| P1H, P2H, P3H, P4H | Pulse width*16 | Tpwh | 1000 | 2000 | - | ns |
| | Rise and fall times*16 | Tprh, Tpfh | 10 | - | - | ns |
| | Pulse overlap time | Tovrh | 500 | 1000 | - | ns |
| | Duty ratio*16 | - | 40 | 50 | 60 | % |
| SG | Pulse width*16 | Tpws | 1000 | 2000 | - | ns |
| | Rise and fall times*16 | Tprs, Tpfs | 10 | - | - | ns |
| | Pulse overlap time | Tovrh | 500 | 1000 | - | ns |
| | Duty ratio*16 | - | 40 | 50 | 60 | % |
| RG | Pulse width | Tpwr | 100 | 1000 | - | ns |
| | Rise and fall times | Tprr, Tpfrr | 5 | - | - | ns |
| TG-P1H | Overlap time | Tovr | 1 | 2 | - | µs |

*16: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm, tolerance unless otherwise noted: ± 0.15)



Unless otherwise noted: ± 0.15
 *1: Glass thickness (refractive index ≈ 1.5)
 *2: Distance from package bottom to photosensitive surface
 Weight: 9 g

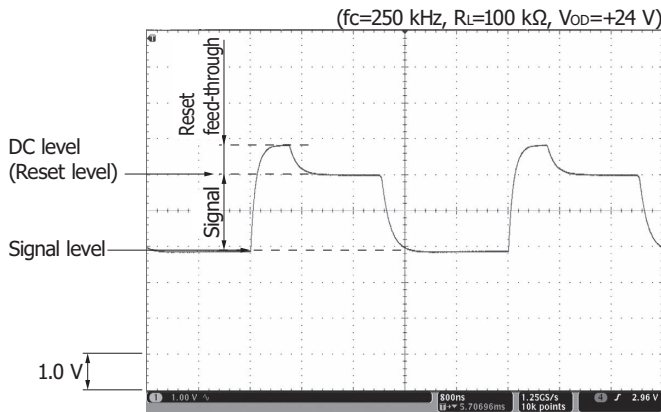
| Type no. | A | B |
|-------------|-----------------------|-----------------|
| S16011-1006 | 14.336 \times 0.896 | 11.83 \pm 0.3 |
| S16011-1106 | 28.672 \times 0.896 | 4.67 \pm 0.3 |

KMPDA0632EA

Pin connections

| Pin no. | Symbol | Function | Remark (standard operation) |
|---------|--------|--------------------------------------|-----------------------------|
| 1 | OS | Output transistor source | RL=100 kΩ |
| 2 | OD | Output transistor drain | +24 V |
| 3 | OG | Output gate | +5 V |
| 4 | SG | Summing gate | Same timing as P4H |
| 5 | SS | Substrate | GND |
| 6 | RD | Reset drain | +12 V |
| 7 | Th1 | Thermistor | |
| 8 | P- | TE-cooler- | |
| 9 | P4H | CCD horizontal register clock-4 | |
| 10 | P3H | CCD horizontal register clock-3 | |
| 11 | P2H | CCD horizontal register clock-2 | |
| 12 | P1H | CCD horizontal register clock-1 | |
| 13 | IG2H | Test point (horizontal input gate-2) | -8 V |
| 14 | IG1H | Test point (horizontal input gate-1) | -8 V |
| 15 | OFG | Overflow gate | +12 V |
| 16 | OFD | Overflow drain | +12 V |
| 17 | ISH | Test point (horizontal input source) | Connect to RD |
| 18 | ISV | Test point (vertical input source) | Connect to RD |
| 19 | SS | Substrate | GND |
| 20 | RD | Reset drain | +12 V |
| 21 | P+ | TE-cooler+ | |
| 22 | Th2 | Thermistor | |
| 23 | IG2V | Test point (vertical input gate-2) | -8 V |
| 24 | IG1V | Test point (vertical input gate-1) | -8 V |
| 25 | P2V | CCD vertical register clock-2 | |
| 26 | P1V | CCD vertical register clock-1 | |
| 27 | TG | Transfer gate | Same timing as P2V |
| 28 | RG | Reset gate | |

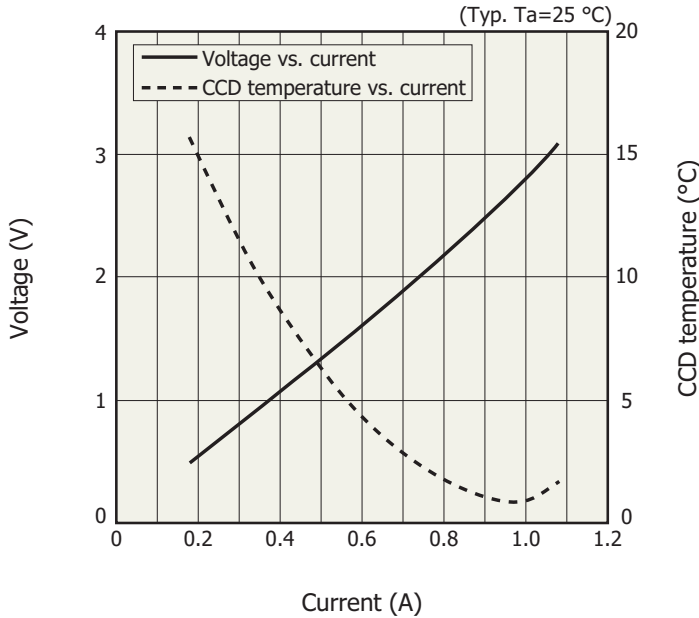
OS output waveform example



Specifications of built-in TE-cooler (Typ., vacuum condition)

| Parameter | Symbol | Condition | Specification | Unit |
|--|------------------|-----------------------|---------------|------|
| Internal resistance | R _{int} | T _a =25 °C | 1.6 | Ω |
| Maximum heat absorption ^{*17} | Q _{max} | | 4.0 | W |

*17: This is a theoretical heat absorption level that offsets the temperature difference in the thermoelectric cooler when the maximum current is supplied to the unit.



KMPDB0469EA

Specifications of built-in temperature sensor

A thermistor chip is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R_{T1} = R_{T2} \times \exp \left(\frac{B}{T_1/T_2} \left(\frac{1}{T_1} - \frac{1}{T_2} \right) \right)$$

R_{T1}: Resistance at absolute temperature T₁ [K]

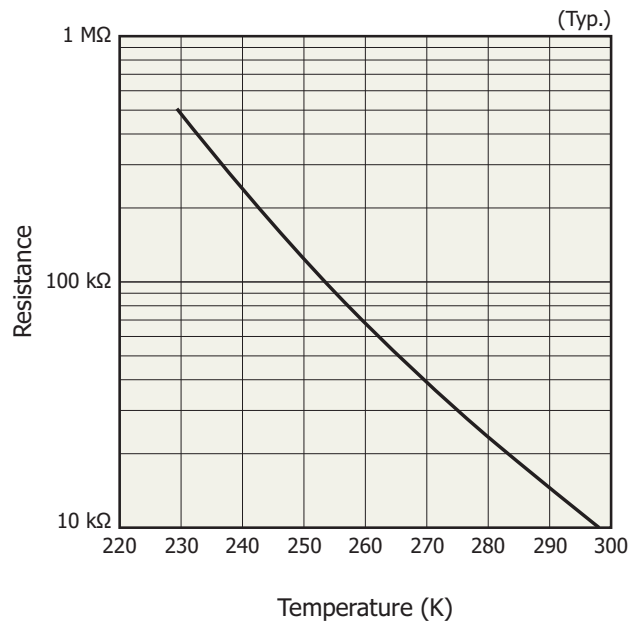
R_{T2}: Resistance at absolute temperature T₂ [K]

B_{T1/T2}: B constant [K]

The characteristics of the thermistor used are as follows.

R₂₉₈=10 kΩ

B_{298/323}=3900 K



KMPDB00470EA

Recommended soldering conditions

| Parameter | Specification | Remark |
|--------------------|-----------------------------------|--------------------------------------|
| Solder temperature | 260 °C max. (once, less than 5 s) | at least 1.8 mm away from lead roots |

Precautions

- If the thermoelectric cooler does not radiate away sufficient heat, then the product temperature will rise and cause physical damage or deterioration to the product. Make sure there is sufficient heat dissipation during cooling. As a heat dissipation measure, we recommend applying a high heat-conductivity material (silicone grease, etc.) over the entire area between the product and the heat-sink (metallic block, etc.), and screwing and securing the product to a heatsink.
- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

- Disclaimer
- Image sensors

■ Technical information

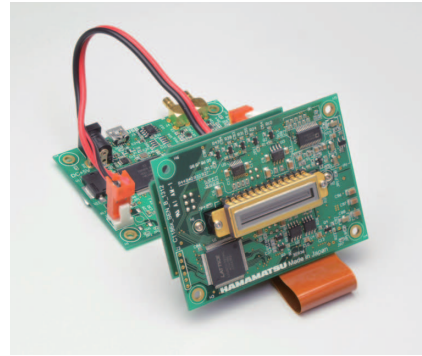
- FFT-CCD area image sensor

Driver circuit C11860 (sold separately) for CCD image sensor (S11850-1106, S11511/S14651 series)

The C11860 is a driver circuit developed for the Hamamatsu CCD image sensor S11511/S14651 series and S11850-1106.

Features

- Built-in 16-bit A/D converter
- The sensor circuit board and interface circuit board are connected using a flexible cable.
- Interface: USB 2.0
- External synchronization capable
- Single power supply: +5 VDC
- Sensor cooling control (approx. +5 °C)



Information described in this material is current as of September 2020.

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