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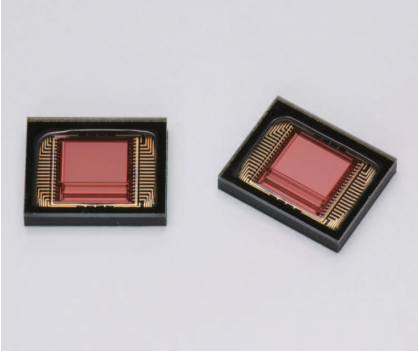
Distance area image sensor



S11963-01CR

Measures the distance to an object by TOF (Time-Of-Flight) method

The distance image sensors are designed to measure the distance to an object by TOF method. When used in combination with a pulse modulated light source, this sensor outputs phase difference information on the timing that the light is emitted and received. The sensor output signals are arithmetically processed by an external signal processing circuit or a PC to obtain distance data.

Features

- **High-speed charge transfer structure**
- **Wide dynamic range, low noise by non-destructive readout**
- **Built-in column gain amplifier (gain: 1, 2 or 4 times)**
- **Operates with minimal detection errors even under fluctuating (charge drain function)**
- **Real-time distance measurement**

Applications

- **Obstacle detection (self-driving, robots, etc.)**
- **Security (intrusion detection, etc.)**
- **Shape recognition (logistics, robots, etc.)**
- **Motion capture**

Structure

Parameter	Specification	Unit
Image size	4.8 × 3.6	mm
Pixel size	30 × 30	μm
Pixel pitch	30	μm
Number of pixels	168 × 128	pixels
Number of effective pixels	160 × 120	pixels
Package	44-pin PWB	-
Window material	AR-coated glass	-

Note: This product is not hermetically sealed.

Absolute maximum ratings

Parameter		Symbol	Condition	Value	Unit
Analog supply voltage		Vdd(A)	Ta=25 °C	-0.3 to +6	V
Digital supply voltage		Vdd(D)	Ta=25 °C	-0.3 to +6	V
Analog input terminal voltage	Pixel reset	Vr	Ta=25 °C	-0.3 to Vdd(A) + 0.3	V
	Output offset	Vref			
	Column gain circuit	Vref2			
	Gain selection	sel0, sel1, sel2			
	Photosensitive area	Vpg			
Digital input terminal voltage	Frame reset pulse	reset	Ta=25 °C	-0.3 to Vdd(D) + 0.3	V
	Frame synchronous trigger pulse	vst			
	Line synchronous trigger pulse	hst			
	Pixel reset pulse	ext_res			
	Master clock pulse	mclk			
Charge transfer clock pulse voltage		VTX1, VTX2, VTX3	Ta=25 °C	-0.3 to Vdd(A) + 0.3	V
Operating temperature		Topr	No dew condensation*1	-25 to +85	°C
Storage temperature		Tstg	No dew condensation*1	-40 to +100	°C
Reflow soldering conditions*2		Tsol		260 °C max. 2 times (see P.10)	-

*1: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*2: JEDEC level 3
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Analog supply voltage		Vdd(A)	4.75	5	5.25	V
Digital supply voltage		Vdd(D)	4.75	5	5.25	V
Bias voltage	Pixel reset	Vr	3.7	3.9	4.1	V
	Output offset	Vref	2.3	2.5	2.7	V
	Column gain amplifier	Vref2	2.5	2.7	2.9	V
	Photosensitive area	Vpg	0.8	1.0	1.2	V
Frame reset pulse voltage	High level	reset	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Frame synchronous trigger pulse voltage	High level	vst	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Line synchronous trigger pulse voltage	High level	hst	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Master clock pulse voltage	High level	mclk	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Pixel reset pulse voltage	High level	ext_res	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Output signal effective period pulse voltage	High level	oe	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Output signal synchronous pulse voltage	High level	dclk	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Non-readout period pulse voltage	High level	dis_read	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Gain selection terminal voltage	High level	sel0, sel1, sel2	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	

Electrical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=5 V]

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse frequency	f(mclk)		1 M	-	10 M	Hz
Video data rate	DR		-	f(mclk)	-	Hz
Current consumption	Ic	Dark state	-	15	30	mA

Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=5 V, Vref2=2.7 V, Vref=2.5 V, Vr=3.9 V, MCLK=10 MHz, Gain: 1 time]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	λ		400 to 1100		nm
Peak sensitivity wavelength	λp	-	800	-	nm
Photosensitivity*3	S	3.0×10^{12}	6.0×10^{12}	1.2×10^{13}	V/W·s
Dark output	Vd	-	1	10	V/s
Random noise	RN	-	0.5	1	mV rms
Dark output voltage*4	Vor	2.6	-	4.3	V
Saturation output voltage	Vsat	1.3	-	2.7	V
Sensitivity ratio*5	SR	0.7	-	1.43	-
Photoresponse nonuniformity*6	PRNU	-	-	±10	%
Number of defective pixels	-	-	-	19	-

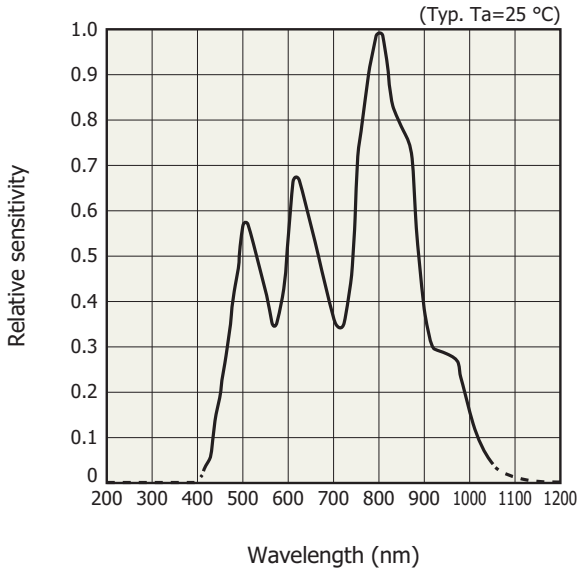
*3: Monochromatic wavelength source (λ=805 nm)

*4: Output voltage right after reset in dark state

*5: Sensitivity ratio of Vout1 (VTX1=3 V, VTX2=VTX3=0 V) and Vout2 (VTX2=3 V, VTX1=VTX3=0 V)

*6: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by white light which is approx. 50% of the saturation level. PRNU is measured using the pixels excluding the pixels of the 4 outermost lines and defective pixels, and is defined as follows:
PRNU= ΔX/X × 100 (%)
X: average output of all pixels, ΔX: standard deviation of pixel output

Spectral response



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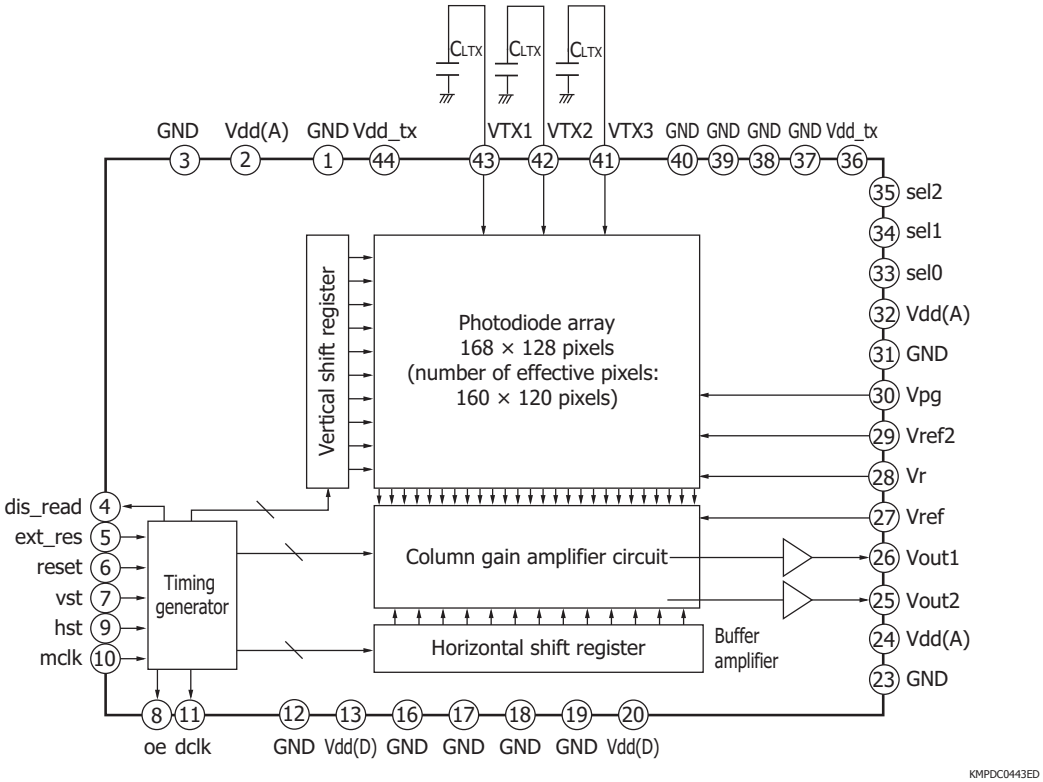
Block diagram



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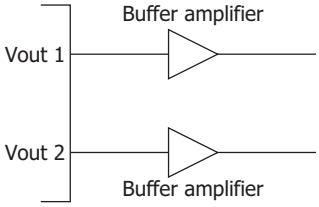
Basic connection example



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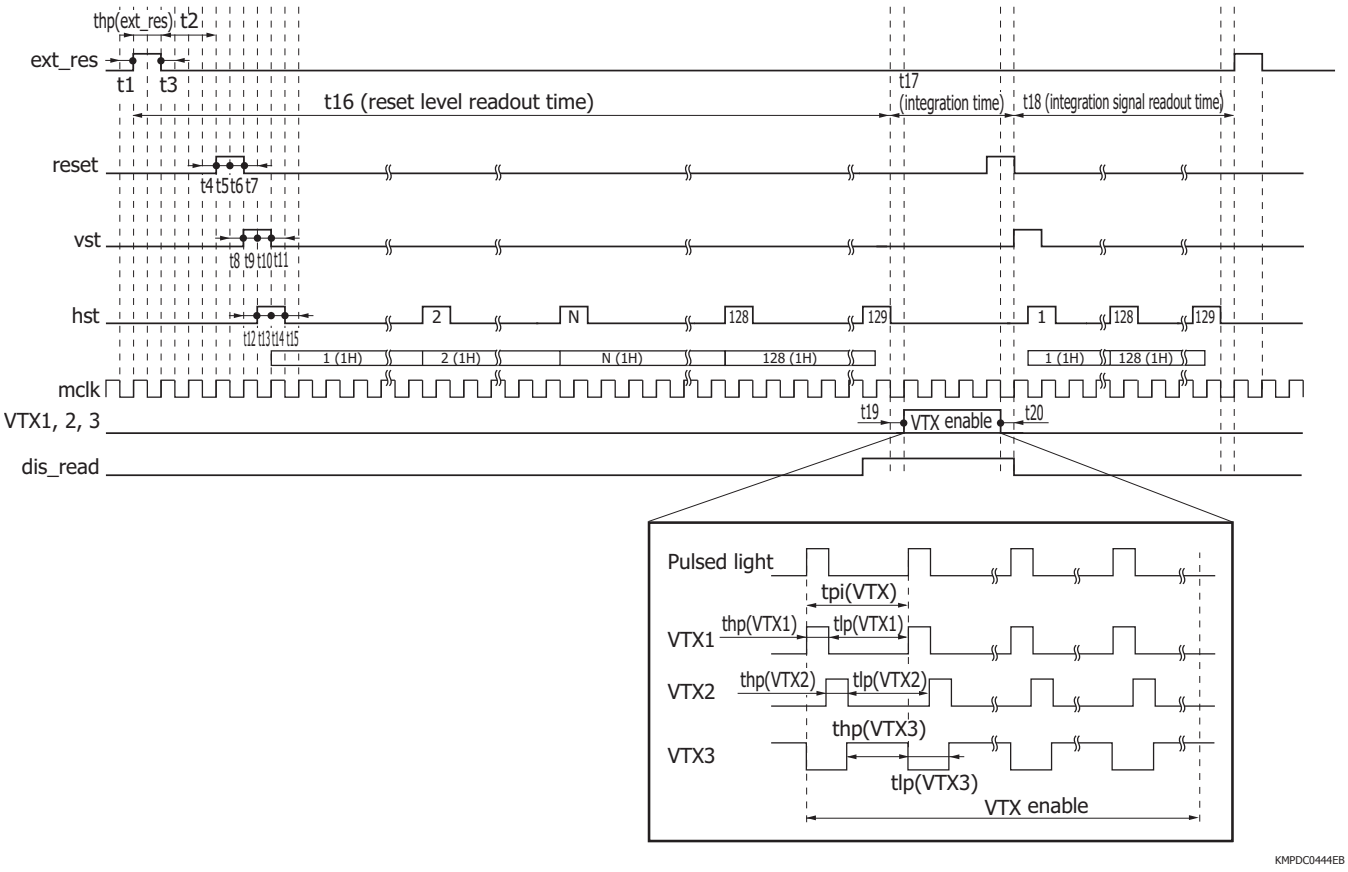
Timing chart

Frame timing



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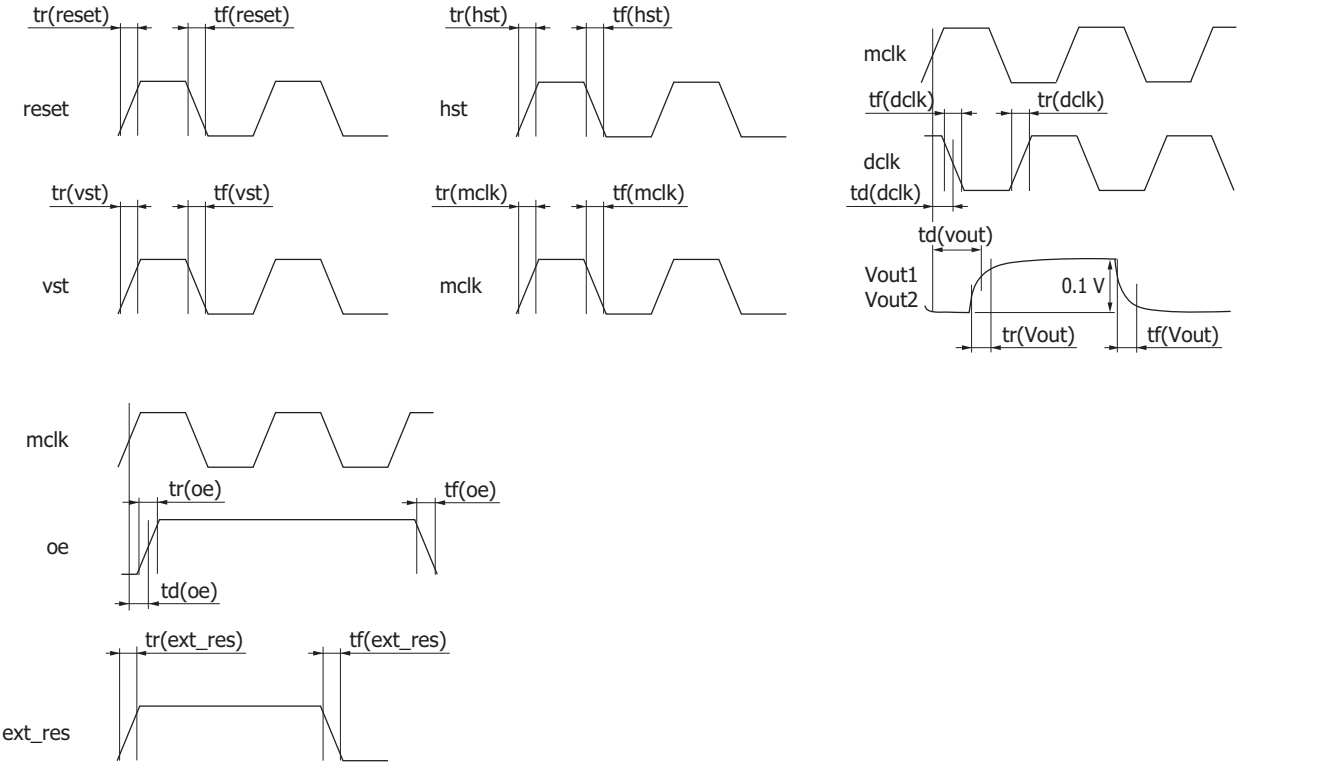

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Calculation method of frame rate

Frame rate=1/(Time per frame)
=1/(Integration time + Readout time)

Integration time:
It is necessary to be changed by the required distance accuracy and usage environment factors such as fluctuating background light.

$$\text{Readout time}=\frac{1}{\text{Clock pulse frequency}} \times \text{Horizontal timing clock} \times \text{Number of vertical pixels}$$

=Time per clock (Readout time per pixel) × Horizontal timing clocks × Number of vertical pixels

Calculation example of readout time (clock pulse frequency: 5 MHz, horizontal timing clocks: 208, number of vertical pixels: 128)

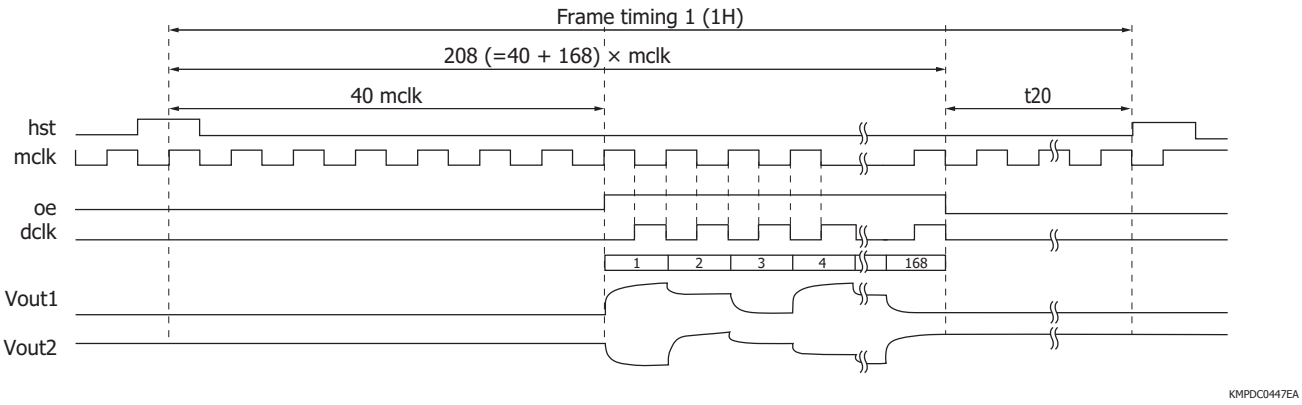
$$\text{Readout time}=\frac{1}{5 \times 10^6\,[\text{Hz}]} \times 208 \times 128$$

=200 [ns] × 208 × 128
=5.324 [ms]

When operating in non-destructive readout mode:
Time per frame = Integration time + (Readout time × Non-destructive readout count)

It is possible to read out only the signal level without reading out the rest level signal. However, noise will increase because the pixel reset noise cannot be removed. Sensitivity variations in the photosensitive area will also increase because the fixed pattern noise in each pixel cannot be removed either.

■ Horizontal timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
Master clock pulse duty ratio	-	45	50	55	%
Master clock pulse rise and fall times	tr(mclk), tf(mclk)	0	-	20	ns
Frame reset pulse rise and fall times	tr(reset), tf(reset)	0	-	20	ns
Frame synchronous trigger pulse rise and fall times	tr(vst), tf(vst)	0	-	20	ns
Line synchronous trigger pulse rise and fall times	tr(hst), tf(hst)	0	-	20	ns
Pixel reset pulse high period	thp(ext_res)	10	-	-	µs
Pixel reset pulse rise and fall times	tr(ext_res), tf(ext_res)	0	-	20	ns
Time from falling edge of master clock pulse to rising edge of pixel reset pulse	t1	1/4 × 1/f(mclk)	-	-	s
Time from rising edge of pixel reset pulse to falling edge of frame reset pulse	t2	0	-	-	s
Time from falling edge of pixel reset pulse to falling edge of master clock pulse	t3	1/4 × 1/f(mclk)	-	-	s
Time from falling edge of master clock pulse to rising edge of frame reset pulse	t4	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of frame reset pulse to falling edge of master clock pulse	t5	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of master clock pulse to falling edge of frame reset pulse	t6	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of frame reset pulse to falling edge of master clock pulse	t7	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of master clock pulse to rising edge of frame synchronous trigger pulse	t8	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of frame synchronous trigger pulse to falling edge of master clock pulse	t9	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of master clock pulse to falling edge of frame synchronous trigger pulse	t10	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of frame synchronous trigger pulse to falling edge of master clock pulse	t11	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of master clock pulse to rising edge of line synchronous trigger pulse	t12	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of line synchronous trigger pulse to rising edge of master clock pulse	t13	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of master clock pulse to falling edge of line synchronous trigger pulse	t14	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of line synchronous trigger pulse to rising edge of master clock pulse	t15	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Reset level readout time	t16	{208/f(mclk) + t20} × 128 + thp(ext_res) + t3	-	-	s
Integration time	t17	-	10	-	ms
Integration signal readout time	t18	{208/f(mclk) + t20} × 128 + {1/2 × 1/f(mclk)}	-	-	s
Time from falling edge of line synchronous pulse (last pulse) to "VTX enable period=on"	t19	0			s
Time from "VTX enable period=off" to falling edge of frame reset pulse	t20	0			s
Time from rising edge of master clock pulse (after reading from all pixels) to rising edge of master clock pulse (hst: High period)	t21	10/f(mclk)			s
Time from falling edge of master clock pulse to rising edge of output signal synchronous pulse*7	td(dclk)	0	25	50	ns
Rise time of output signal synchronous pulse output voltage (10 to 90%)*7	tf(dclk)	-	20	40	ns
Fall time of output signal synchronous pulse output voltage (10 to 90%)*7	tf(dclk)	-	20	40	ns

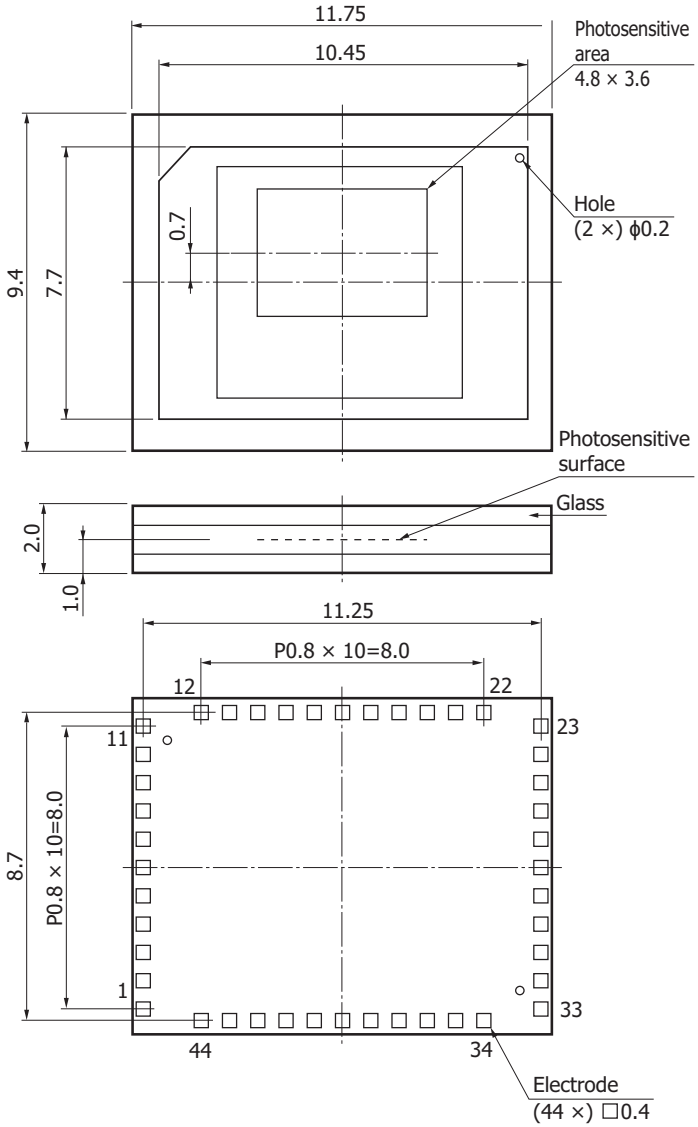
Parameter		Symbol	Min.	Typ.	Max.	Unit
Time from rising edge of master clock pulse to rising edge of output signal effective period pulse*7		td(oe)	0	25	50	ns
Output signal effective period pulse rise time (10 to 90%)*7		tr(oe)	-	20	40	ns
Output signal effective period pulse fall time (10 to 90%)*7		tf(oe)	-	20	40	ns
Settling time of output signal 1, 2 (10 to 90%)*7 *8		tr(Vout), tf(Vout)	-	35	70	ns
Time from rising edge of master clock pulse to output signal 1, 2 (output 50%)*7		td(Vout)	-	40	80	ns
Charge transfer clock pulse interval		tpi(VTX)	60	-	-	ns
Charge transfer clock pulse (VTX1) high period		thp(VTX1)	30	-	-	ns
Charge transfer clock pulse (VTX1) low period		tlp(VTX1)	-	tpi(VTX) - thp(VTX2) - thp(VTX3)	-	ns
Charge transfer clock pulse (VTX2) high period		thp(VTX2)	30	-	-	ns
Charge transfer clock pulse (VTX2) low period		tlp(VTX2)	-	tpi(VTX) - thp(VTX1) - thp(VTX3)	-	ns
Charge transfer clock pulse (VTX3) high period		thp(VTX3)	0	-	-	ns
Charge transfer clock pulse (VTX3) low period		tlp(VTX3)	-	tpi(VTX)- thp(VTX1)- thp(VTX2)	-	ns
Charge transfer clock pulse voltage rise time		tr(VTX)	-	3	-	ns
Charge transfer clock pulse voltage fall time		tf(VTX)	-	3	-	ns
Charge transfer clock pulse voltage	High level	VTX1, VTX2, VTX3	-	3	-	V
	Low level		-	0	-	
Time from rising edge of line synchronous trigger pulse to rising edge of non-readout period pulse*7		td(dis_read)	-	25	50	ns
Non-readout period pulse rise time (10 to 90%)*7		tr(dis_read)	-	20	40	ns
Non-readout period pulse fall time (10 to 90%)*7		tf(dis_read)	-	20	40	ns

*7: C_L=3 pF
*8: Output voltage=0.1 V

Input terminal capacitance (Ta=25 °C, Vdd=5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Charge transfer clock pulse internal load capacitance	C_{LTX}	-	40	-	pF

Dimensional outline (unit: mm)



Tolerance unless otherwise noted: ±0.2, ±2°

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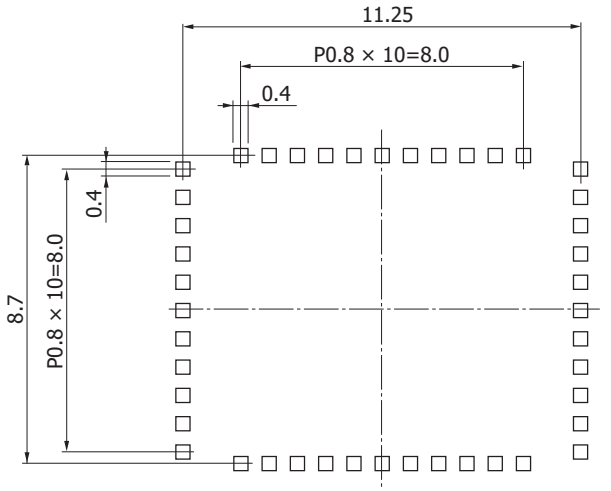
Recommended land pattern (unit: mm)



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Pin connections

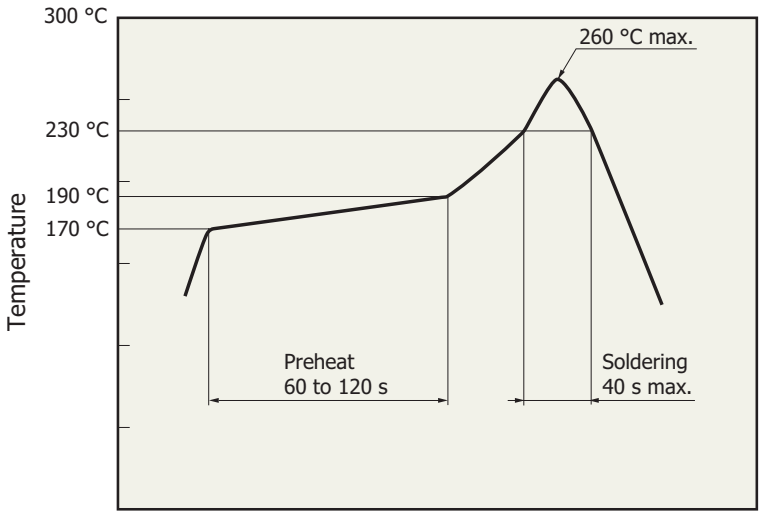
Pin no.	Symbol	I/O	Description
1	GND	I	Ground
2	Vdd(A)	I	Analog supply voltage
3	GND	I	Ground
4	dis_read	O	Non-readout period pulse
5	ext_res	I	Pixel reset pulse
6	reset	I	Frame reset pulse
7	vst	I	Frame synchronous trigger pulse
8	oe	O	Output signal effective period pulse
9	hst	I	Line synchronous trigger pulse
10	mclk	I	Master clock pulse
11	dclk	O	Output signal synchronous pulse
12	GND	I	Ground
13	Vdd(D)	I	Digital supply voltage
14	NC	-	No connection
15	NC	-	No connection
16	GND	I	Ground
17	GND	I	Ground
18	GND	I	Ground
19	GND	I	Ground
20	Vdd(D)	I	Digital supply voltage
21	NC	-	No connection
22	NC	-	No connection
23	GND	I	Ground
24	Vdd(A)	I	Analog supply voltage
25	Vout2	O	Output signal 2
26	Vout1	O	Output signal 1
27	Vref	I	Bias voltage (output offset)
28	Vr	I	Bias voltage (pixel reset)
29	Vref2	I	Bias voltage (column gain circuit)
30	Vpg	I	Bias voltage (photosensitive area)
31	GND	I	Ground
32	Vdd(A)	I	Analog supply voltage
33	sel0	I	Gain selection
34	sel1	I	Gain selection
35	sel2	I	Gain selection
36	Vdd_tx	I	Supply voltage for internal driver circuit of charge transfer clock pulse
37	GND	I	Ground
38	GND	I	Ground
39	GND	I	Ground
40	GND	I	Ground
41	VTX3	I	Charge transfer clock pulse 3
42	VTX2	I	Charge transfer clock pulse 2
43	VTX1	I	Charge transfer clock pulse 1
44	Vdd_tx	I	Supply voltage for internal driver circuit of charge transfer clock pulse

Note: Leave "NC" terminals open and do not connect them to GND.
Connect impedance convering buffer amplifiers to Vout1/Vout2 so as to minimize the current flow.

Gain setting

Gain	sel0	sel1	sel2
1	H	H	H
2	H	L	L
4	L	H	L

Measured example of temperature profile with hot-air reflow oven for product testing



- This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 168 hours.
- The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. Before actual reflow soldering, check for any problems by testing out the reflow soldering methods in advance.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions

- Disclaimer
- Surface mount type products
- Image sensors

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