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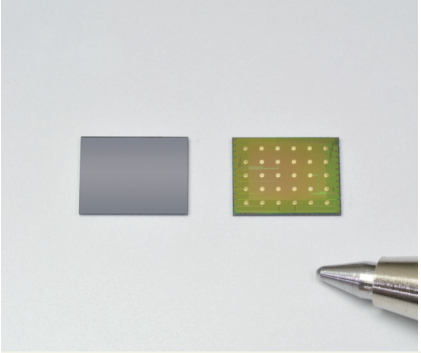
NEW

Distance area image sensor



S15454-01WT

Back-thinned type, measures the distance to an object by TOF method

The distance image sensor is designed to measure the distance to an object by TOF (time-of-flight) method. When used in combination with a pulse modulated light source, this sensor outputs phase difference information on the timing that the light is emitted and received. Distance data can be obtained by performing calculation on the output signal with an external signal processing circuit or on a PC. We provide an evaluation kit for this product. Contact us for detailed information.

Features

- **High sensitivity in the near infrared region**
- **Improved tolerance to background light**
- **Compact wafer level package (WLP) type**

Applications

- **Obstacle detection (self-driving, robots, etc.)**
- **Security (intrusion detection, etc.)**
- **Shape recognition (logistics, robots, etc.)**
- **Motion capture**
- **Touchless operation**

Structure

Parameter	Specification	Unit
Image size	4.8 × 3.6	mm
Pixel size	50 × 50	μm
Pixel pitch	50	μm
Number of pixels	104 × 80	pixels
Number of effective pixels	96 × 72	pixels
Package	WLP	-

Note: This product is not hermetically sealed.

Absolute maximum ratings

Parameter		Symbol	Condition	Value	Unit
Analog supply voltage		Vdd(A)	Ta=25 °C	-0.3 to +4.2	V
Digital supply voltage		Vdd(D)	Ta=25 °C	-0.3 to +4.2	V
Analog input terminal voltage	Pixel reset	Vr	Ta=25 °C	-0.3 to Vdd(A) + 0.3	V
	VTX power supply	Vdd(VTX)			
	Photosensitive area	Vpg			
Digital input terminal voltage	Frame reset pulse	reset	Ta=25 °C	-0.3 to Vdd(D) + 0.3	V
	Frame sync trigger pulse	vst			
	Line sync trigger pulse	hst			
	Pixel reset pulse	ext_reset			
	Master clock pulse	mclk			
Charge transfer clock pulse voltage		VTX1, VTX2, VTX3	Ta=25 °C	-0.3 to Vdd(A) + 0.3	V
Operating temperature		Topr	No dew condensation*1	-25 to +85	°C
Storage temperature		Tstg	No dew condensation*1	-40 to +85	°C
Soldering temperature*2		Tsol		245 (twice)	°C

*1: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.
*2: Reflow soldering, IPC/JEDEC J-STD-020 MSL 2, see P.10
Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.

Recommended terminal voltage (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Analog supply voltage		Vdd(A)	3.2	3.3	3.4	V
Digital supply voltage		Vdd(D)	3.2	3.3	3.4	V
Bias voltage	Pixel reset	Vr	2.5	2.6	2.7	V
	VTX power supply	Vdd(VTX)	1.6	1.8	2.0	V
	Photosensitive area	Vpg	0.6	0.8	1.0	V
Frame reset pulse voltage	High level	reset	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Frame sync trigger pulse voltage	High level	vst	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Line sync trigger pulse voltage	High level	hst	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Master clock pulse voltage	High level	mclk	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Pixel reset pulse voltage	High level	ext_reset	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	
Output signal sync pulse voltage	High level	dclk	Vdd(D) × 0.8	-	-	V
	Low level		-	-	Vdd(D) × 0.2	

Electric characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V]

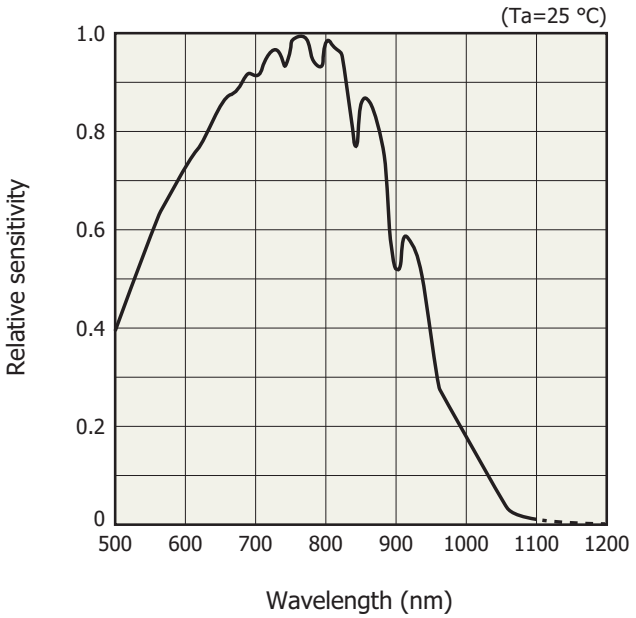
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse frequency	f(mclk)		1 M	-	10 M	Hz
Data rate	DR		-	f(mclk)	-	Hz
Current consumption	Ic	Dark state	-	6	-	mA

Electrical and optical characteristics [Ta=25 °C, Vdd(A)=Vdd(D)=3.3 V, Vr=2.6 V, MCLK=10 MHz]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Spectral response range	λ		500 to 1100		nm
Peak sensitivity wavelength	λp	-	800	-	nm
Photosensitivity*3	S	-	1×10^{12}	-	$V/W \cdot s \cdot m^2$
Dark output	Vd	-	2.8	-	V/s
Random noise	RN	-	0.5	-	mV rms
Dark output voltage*4	Vor	-	2.35	-	V
Sensitivity ratio*5	SR	0.7	-	1.43	-
Photoresponse nonuniformity*6	PRNU	-	-	±10	%

*3: Monochromatic wavelength light source (λ=805 nm)
*4: Output value right after reset in dark state
*5: Output ratio of Vout1 (VTX1=1.8 V, VTX2=VTX3=0 V) to Vout2 (VTX2=1.8 V, VTX1=VTX3=0 V)
*6: Photoresponse nonuniformity (PRNU) is the output nonuniformity that occurs when the entire photosensitive area is uniformly illuminated by light which is 50% of the saturation exposure level. PRNU is measured using 64 pixels excluding 8 pixels each at both ends, and is defined as follows.
PRNU=(ΔX/X) × 100 [%]
X: average of the output of all pixel, ΔX: difference between the maximum or minimum output and X

Spectral response (typical example)



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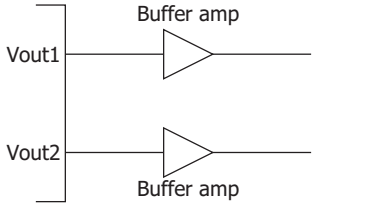
Basic connection example



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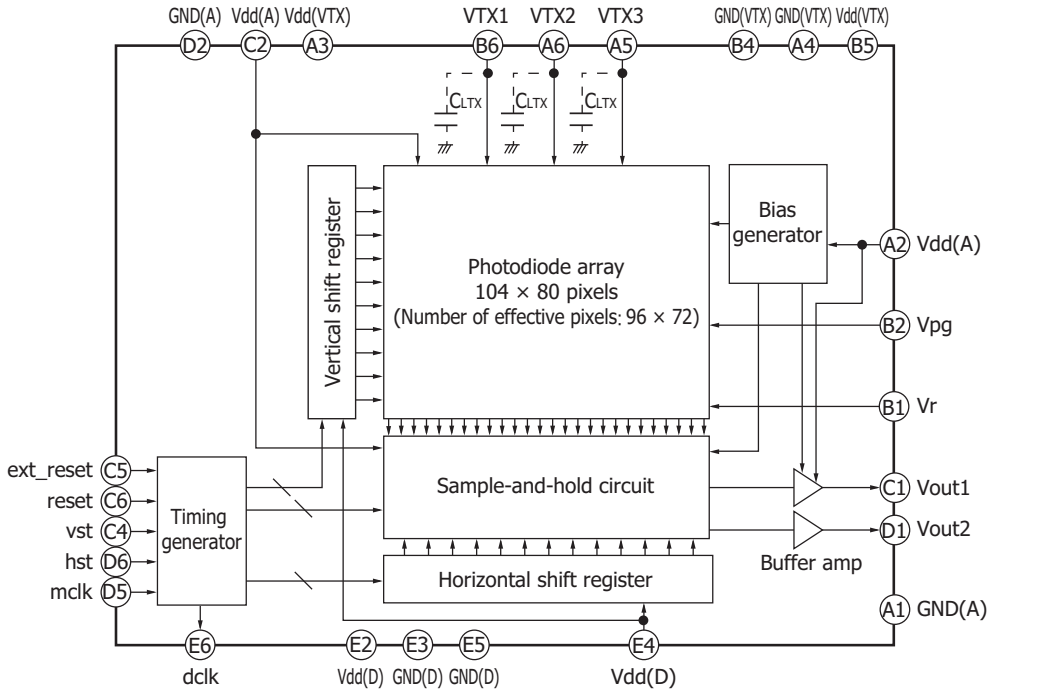
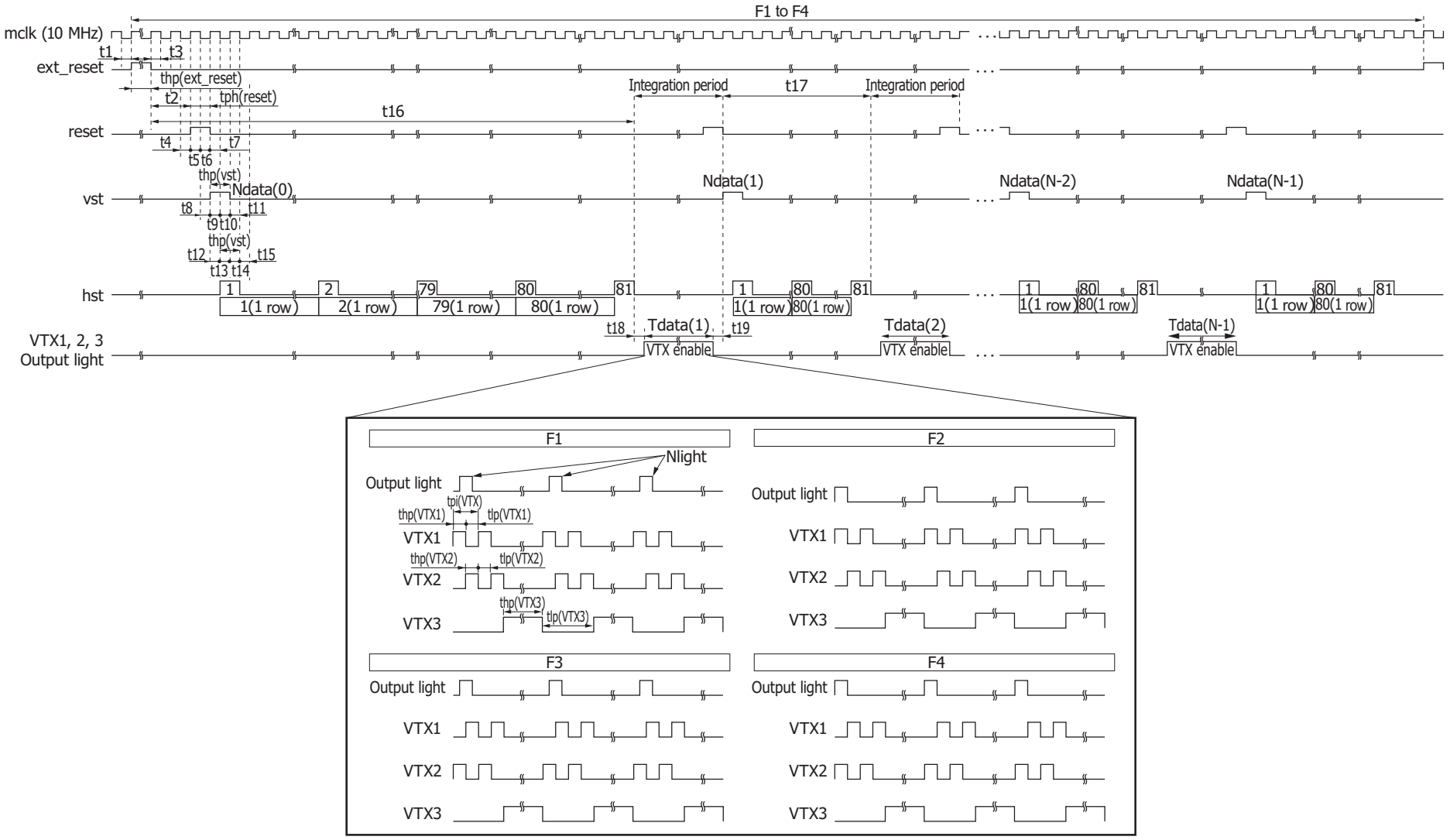
Block diagram



KMPDC0744EB

Timing chart



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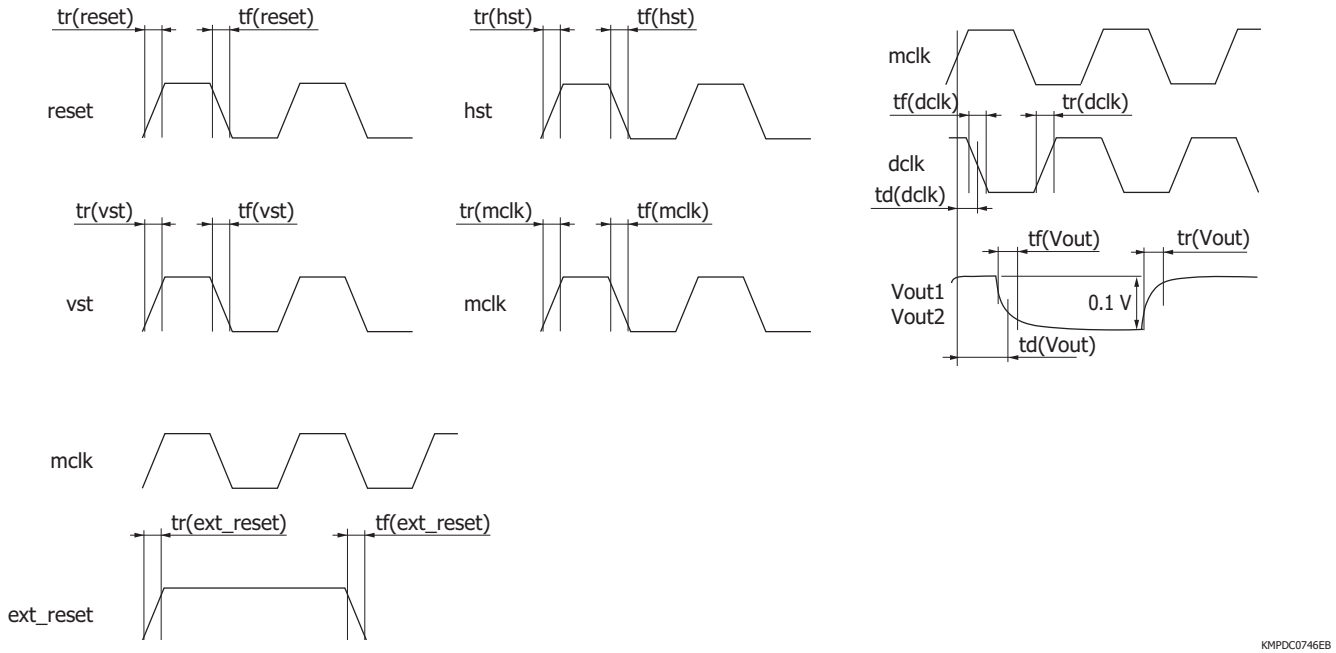


Calculation method of frame rate

Frame rate=1/4 of subframe time
=1/{(Integration time + Readout time) × 4}

■ When operating in non-destructive readout mode
Time per subframe=Integration time + (Readout time × Non-destructive readout count)

Note: The integration time setting needs to be changed depending on the required distance accuracy and usage environment factors such as background light.
Integration signal can be read out without reading out the reset level. But this may increase random noise and degrade sensitivity uniformity of the photosensitive area.

[Readout time calculation]

$$\text{Readout time} = \frac{1}{\text{Clock pulse frequency}} \times \text{Number of horizontal timing clock} \times \text{Number of vertical pixels}$$

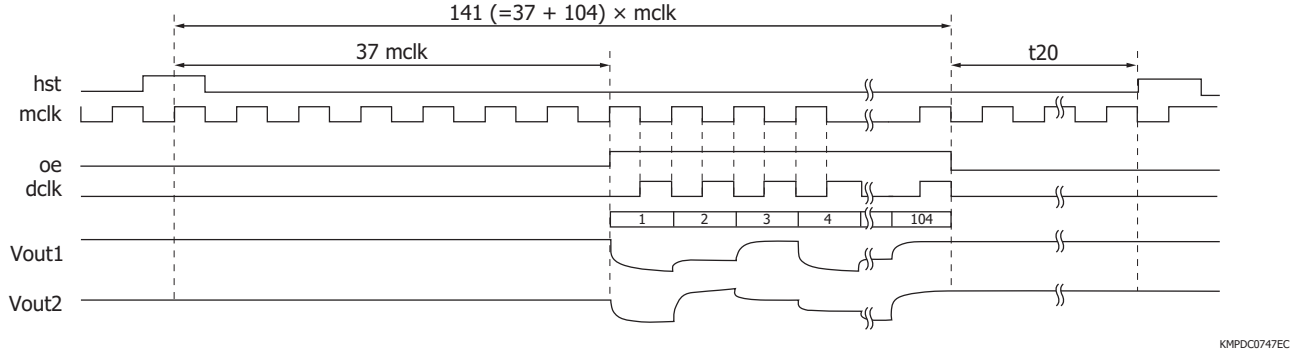
=Time per clock (Readout time per pixel) × Number of horizontal timing clock × Number of vertical pixels

· Calculation example [clock pulse frequency=10 MHz, number of horizontal timing clock=141 (=37 + 104), number of vertical pixels=80]

$$\text{Readout time} = \frac{1}{5 \times 10^6\ [\text{Hz}]} \times 141 \times 80$$

=100 [ns] × 141 × 80
=1.128 [ms]

■ Horizontal timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
Master clock pulse duty ratio	-	45	50	55	%
Master clock pulse rise and fall times*7	tr(mclk), tf(mclk)	0	-	20	ns
Frame reset pulse rise and fall times*7	tr(reset), tf(reset)	0	-	20	ns
Frame sync trigger pulse rise and fall times*7	tr(vst), tf(vst)	0	-	20	ns
Line sync trigger pulse rise and fall times*7	tr(hst), tf(hst)	0	-	20	ns
Pixel reset pulse high period	thp(ext_reset)	10	-	-	µs
Pixel reset pulse rise and fall times	tr(ext_reset), tf(ext_reset)	0	-	20	ns
Time from falling edge of master clock pulse to rising edge of pixel reset pulse	t1	1/4 × 1/f(mclk)	-	-	s
Time from falling edge of pixel reset pulse to rising edge of frame reset pulse	t2	0	-	-	s
Time from falling edge of pixel reset pulse to falling edge of master clock pulse	t3	1/4 × 1/f(mclk)	-	-	s
Time from falling edge of master clock pulse to rising edge of frame reset pulse	t4	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of frame reset pulse to falling edge of master clock pulse	t5	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of master clock pulse to falling edge of frame reset pulse	t6	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of frame reset pulse to falling edge of master clock pulse	t7	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of master clock pulse to rising edge of frame sync trigger pulse	t8	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of frame sync trigger pulse to falling edge of master clock pulse	t9	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of master clock pulse to falling edge of frame sync trigger pulse	t10	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of frame sync trigger pulse to falling edge of master clock pulse	t11	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of master clock pulse to rising edge of line sync trigger pulse	t12	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of line sync trigger pulse to rising edge of master clock pulse	t13	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from rising edge of master clock pulse to falling edge of line sync trigger pulse	t14	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Time from falling edge of line sync trigger pulse to rising edge of master clock pulse	t15	1/4 × 1/f(mclk)	-	1/2 × 1/f(mclk)	s
Readout time for reset level	t16	{141/f(mclk) + t20} × 80 + thp(ext_res) + t3	-	-	s
Readout time for integration signals	t17	{141/f(mclk) + t20} × 80 + {1/2 × 1/f(mclk)}	-	-	s
Time from line sync trigger pulse (last pulse in a frame) to VTX drive period ON	t18	0	-	-	s
Time from VTX drive period OFF to falling edge of frame reset pulse	t19	0	-	-	s
Time from falling edge of master clock pulse (after reading signals from all pixels) to rising edge of master clock puse (hst: high period)	t20	10/f(mclk)	-	-	s
Time from falling edge of master clock pulse to rising edge of output signal sync pulse*8	td(dclk)	-	12	-	ns
Output signal sync pulse rise time*7 *8	tr(dclk)	-	12	-	ns
Output signal sync pulse fall time*7 *8	tf(dclk)	-	9	-	ns
Settling rise time of output signal 1, 2*7 *8 *9	tr(Vout)	-	15	27	ns
Settling fall time of output signal 1, 2*7 *8 *9	tf(Vout)	-	15	27	ns
Time from rising edge of master clock pulse to output signal 1, 2 (output 50%)*8	td(Vout)	-	20	26	ns

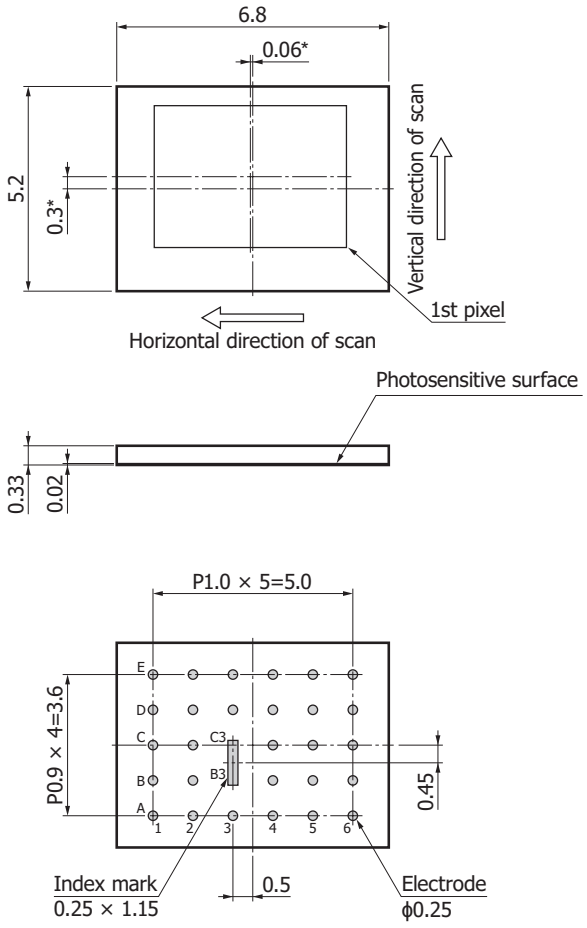
*7: 10 to 90%
*8: Load capacitance C_L=3 pF
*9: Output voltage=0.1 V

Parameter		Symbol	Min.	Typ.	Max.	Unit
Charge transfer clock pulse cycle		tpi(VTX)	60	-	-	ns
Charge transfer clock pulse (VTX1)	High period	thp(VTX1)	30	-	-	ns
	Low period	tlp(VTX1)	-	tpi(VTX) thp(VTX2) thp(VTX3)	-	
Charge transfer clock pulse (VTX2)	High period	thp(VTX2)	30	-	-	ns
	Low period	tlp(VTX2)	-	tpi(VTX) thp(VTX1) thp(VTX3)	-	
Charge transfer clock pulse (VTX3)	High period	thp(VTX3)	0	-	-	ns
	Low period	tlp(VTX3)	-	tpi(VTX) thp(VTX1) thp(VTX2)	-	
Charge transfer clock pulse voltage rise and fall times*7		tr(VTX), tf(VTX)	-	3	-	ns
Charge transfer clock pulse voltage	High level	VTX1, VTX2, VTX3	1.6	1.8	2.0	V
	Low level		-	0	-	

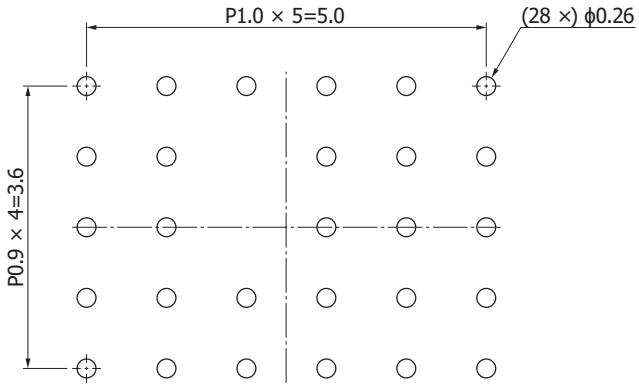
Input terminal capacitance (Ta=25 °C, Vdd=3.3 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Charge transfer clock pulse internal load capacitance	CLTX	-	10	-	pF

Dimensional outline (unit: mm)



Recommended land pattern (unit: mm)



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Tolerance unless otherwise noted: ±0.1
Au electrode
* Distance from package center to photosensitive area center

Pin connections

Pin no.	Symbol	I/O	Description
A1	GND(A)	I	Ground
B1	Vr	I	Pixel reset voltage
C1	Vout1	O	Output signal 1
D1	Vout2	O	Output signal 2
E1	NC	-	No connection
A2	Vdd(A)	I	Analog supply voltage
B2	Vpg	I	Photosensitive area bias voltage
C2	Vdd(A)	I	Analog supply voltage
D2	GND(A)	I	Ground
E2	Vdd(D)	I	Digital supply voltage
A3	Vdd(VTX)	I	Power supply for VTX
B3	NC	-	No connection
C3	NC	-	No connection
D3	NC	-	No connection
E3	GND(D)	I	Ground
A4	GND(VTX)	I	Ground
B4	GND(VTX)	I	Ground
C4	vst	I	Vertical shift register start signal
D4	NC	-	No connection
E4	Vdd(D)	I	Digital supply voltage
A5	VTX3	I	Charge transfer clock 3 (for OFD)
B5	VDD(VTX)	I	Power supply for VTX
C5	ext_reset	I	Vertical shift register reset pulse
D5	mclk	I	Master clock input signal
E5	GND(D)	I	Ground
A6	VTX2	I	Charge transfer clock 2
B6	VTX1	I	Charge transfer clock 1
C6	reset	I	Reset pulse
D6	hst	I	Horizontal shift register start signal
E6	dclk	O	Output data sample clock

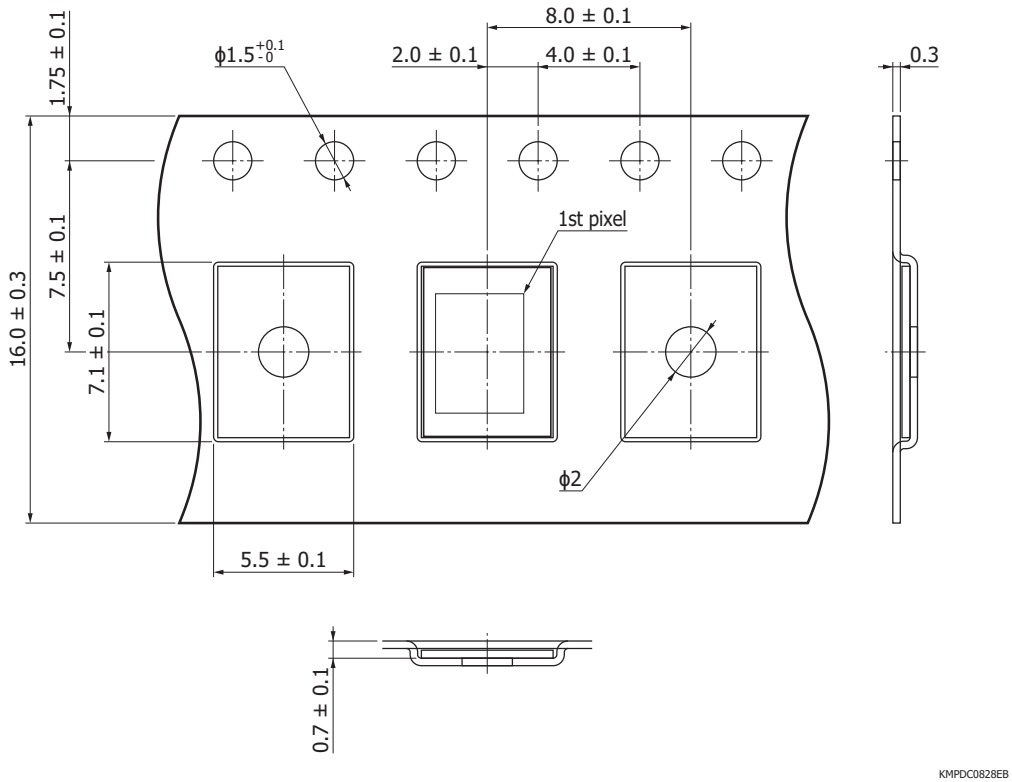
Note: Leave the NC terminals open.
Connect an impedance converting buffer amplifier to Vout1 and Vout2 terminals so as to minimize the current flow.

Reel packing specifications

■ Reel (conforms to JEITA ET-7200)

Outer diameter	Hub diameter	Tape width	Material	Electrostatic characteristics
ϕ180 mm	ϕ60 mm	16 mm	PS	Conductive

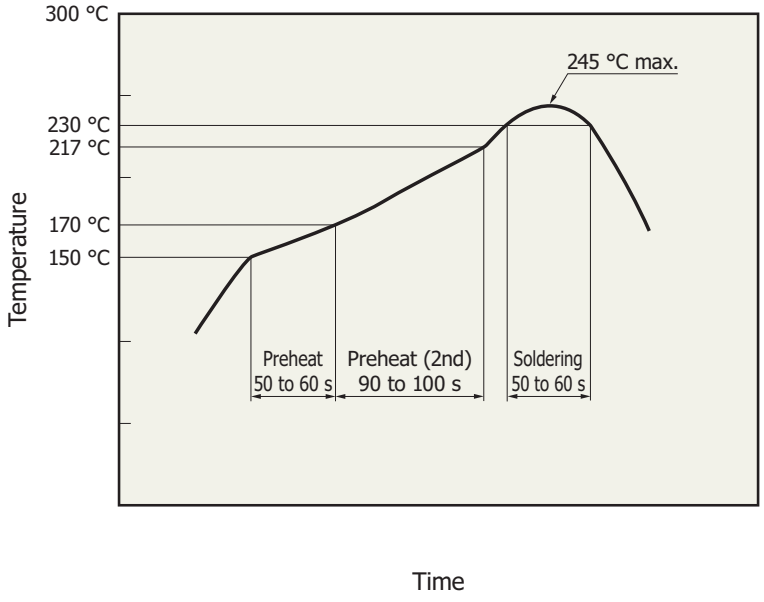
■ Embossed tape (unit: mm, material: PS, conductive)



■ Packing quantity
500 pcs/reel

■ Packing state
Reel and desiccant in moisture-proof packaging (vacuum-sealed)

Recommended soldering conditions



· This product supports lead-free soldering. After unpacking, store it in an environment at a temperature of 30 °C or less and a humidity of 60% or less, and perform soldering within 1 year.
· The effect that the product receives during reflow soldering varies depending on the circuit board and reflow oven that are used. When you set reflow soldering conditions, check that problems do not occur in the product by testing out the conditions in advance.
· In order to improve reliability, we recommend that you use underfill resin to fill the gap between the element and the board, after reflow soldering.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Surface mount type products

■ Technical information
· Distance image sensors (Back-thinned type) S15452/S15453/S15454-01WT

Evaluation kit for distance area image sensor C15359

The evaluation kit [55 mm (H) × 50 mm (V)] is available for the S15454-01WT distance area image sensor (with the S15454-01WT). Contact us for detailed information.

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