TEXAS INSTRUMENTS

LMR16006Y-Q1

SNVSAC1 – JUNE 2015

LMR16006Y-Q1 SIMPLE SWITCHER® Buck Regulators With High-Efficiency ECO Mode

1 Features

- LMR16006Y-Q1 is an Automotive Grade Product that is a AEC-Q100 Grade 1 Qualified (-40°C to +125°C Operating Junction Temperature)
- Input Voltage Range 4 V to 40 V with Transient Up to 65 V
- Output Current up to 600 mA
- 2.1 MHz Switching Frequency
- Ultra Low 28 µA Standby Current in ECO Mode
- 1 µA Shutdown Current
- High Duty Cycle Operation Supported
- ADJ, Fixed 3.3 V and Fixed 5 V Output Option
- Internal Compensation
- High Voltage Enable Input
- Internal Soft Start
- Over Current Protection
- Over Temperature Protection
- Small Overall Solution Size (SOT-6L Package)

2 Applications

- Automotive
- Battery Powered Equipment
- Industrial Distributed Power Systems
- Portable Handheld Instruments
- Portable Media Players
- Aftermarket Automotive Accessories: Video, GPS, Entertainment

3 Description

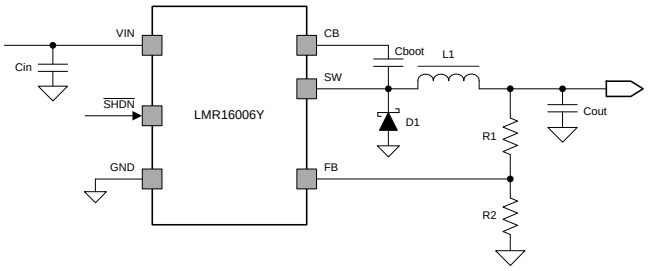
The LMR16006Y-Q1 is a PWM DC-DC buck (step-down) regulator. It is suitable for a wide range of application from industrial to automotive for power conditioning from an unregulated source. The regulator's standby current is 28 µA in ECO mode, which is suitable for battery operating systems. An ultra-low 1 µA shutdown current can further prolong battery life. Operating frequency is fixed at 2.1 MHz allowing the use of small external components while still being able to have low output ripple voltage. Soft-start and compensation circuits are implemented internally, which allows the device to be used with minimized external components. The LMR16006Y-Q1 is optimized for up to 600 mA load currents. It has a 0.765 V typical feedback voltage. The device has built-in protection features such as pulse by pulse current limit, thermal sensing and shutdown due to excessive power dissipation. The LMR16006Y-Q1 is available in a low profile SOT-6L package (2.9 mm x 1.6 mm).

Device Information(1)

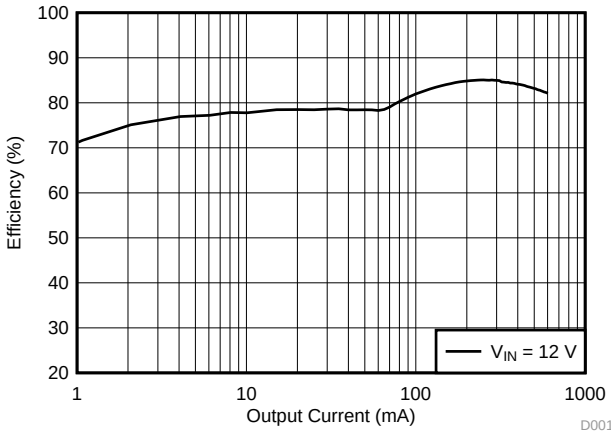
PART NUMBER	PACKAGE	OUTPUT VOLTAGE
LMR16006YQ	SOT (6)	Adjustable
LMR16006YQ3		Fixed 3.3 V
LMR16006YQ5		Fixed 5 V

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Efficiency vs Output Current
(f_{SW}= 2.1 MHz, V_{OUT}= 3.3 V)



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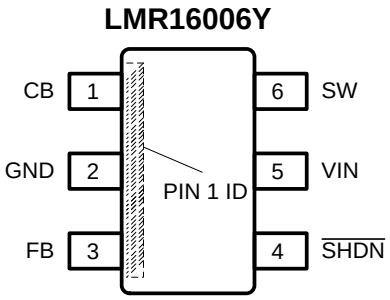
5 Revision History

DATE	REVISION	NOTES
June 2015	*	Initial release.

6 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CB	1	I	Switch FET gate bias voltage. Connect C_{boot} capacitor between CB and SW.
GND	2	G	Ground connection.
FB	3	I	Feedback Input. Set feedback voltage divider ratio with $V_{OUT} = V_{FB}$ (1 + (R1/R2)).
$\overline{SHDN}$	4	I	Enable and disable input (high voltage tolerant). Internal pull-up current source. Pull below 1.25 V to disable. Float to enable. Establish input undervoltage lockout with two resistor divider.
VIN	5	I	Power input voltage pin. Input for internal supply and drain node input for internal high-side MOSFET.
SW	6	O	Switch node. Connect to inductor, diode, and C_{boot} capacitor.

7 Specifications

7.1 Absolute Maximum Ratings (1)

		MIN	MAX	UNIT
Input voltages	V_{IN} to GND	-0.3	65	V
	$\overline{SHDN}$ to GND	-0.3	65	
	FB to GND	-0.3	7	
	CB to SW	-0.3	7	
Output voltages	SW to GND	-1	60	
	SW to GND less than 30 ns transients	-2	60	
T_J Operation junction temperature		-40	150	°C
Storage temperature, T_{stg}		-55	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Buck regulator	V_{IN}	4	40	V
	CB	4	46	
	CB to SW	-0.3	6	
	SW	-1	40	
	FB	0	5.5	
Control	$\overline{SHDN}$	0	40	
Temperature	Operating junction temperature range, T_J	-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC (1)		LMR16006Y-Q1 DDC (SOT) (6 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	36.9	
$R_{\theta JB}$	Junction-to board characterization parameter	28.4	

(1) All numbers apply for packages soldered directly onto a 3" x 3" PC board with 2 oz. copper on 4 layers in still air in accordance to JEDEC standards. Thermal resistance varies greatly with layout, copper thickness, number of layers in PCB, power distribution, numberof thermal vias, board size, ambient temperature, and air flow.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise specified, the following conditions apply: V_{IN} = $\overline{SHDN}$ = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} (INPUT POWER SUPPLY)						
V_{IN}	Operating input voltage		4		40	V
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V		1	3	µA
I_Q	Operating quiescent current (non-switching)	no load, V_{IN} = 12 V		28		µA
UVLO	Undervoltage lockout thresholds	Rising threshold			4	V
		Falling threshold	3			
$\overline{SHDN}$						
V_{SHDN_Thre}	Rising $\overline{SHDN}$ Threshold Voltage		1.05	1.25	1.38	V
I_{SHDN}	Input current	$\overline{SHDN}$ = 2.3 V		-4.2		µA
		$\overline{SHDN}$ = 0.9 V		-1		
I_{SHDN_HYS}	Hysteresis current			-3		µA
HIGH-SIDE MOSFET						
R_{DS_ON}	On-resistance	V_{IN} = 12 V, CB to SW = 5.8 V		900		mΩ
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage		0.747	0.765	0.782	V
V_{OUT}	Output voltage	Fixed 3.3 V output version	3.201	3.3	3.399	V
		Fixed 5 V output version	4.85	5	5.15	V
CURRENT LIMIT						
I_{LIMIT}	Peak current limit	V_{IN} = 12 V, T_J = 25°C		1200	1700	mA
THERMAL PERFORMANCE						
T_{SHDN} (1)	Thermal shutdown threshold			170		ºC
T_{HYS} (1)	Hysteresis			10		ºC

(1) Ensured by design.

7.6 Switching Characteristics

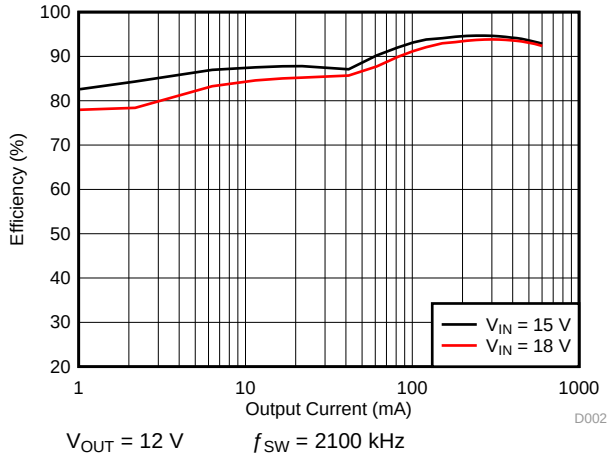
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SW (SW PIN)						
f_{SW}	Switching frequency		1785	2100	2415	kHz
T_{ON_MIN} (1)	Minimum turn-on time	f_{SW} = 2.1 MHz		80		ns
D_{MAX}	Maximum duty cycle			97%		

(1) Ensured by design.

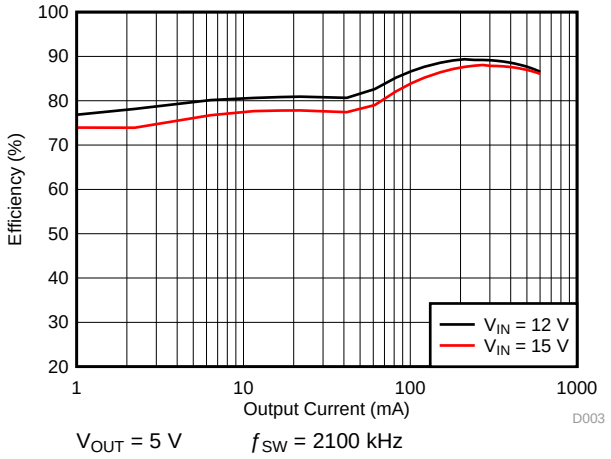
7.7 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 2100 kHz, L1 = 6.8 µH, Cout = 10 µF, T_A = 25°C.



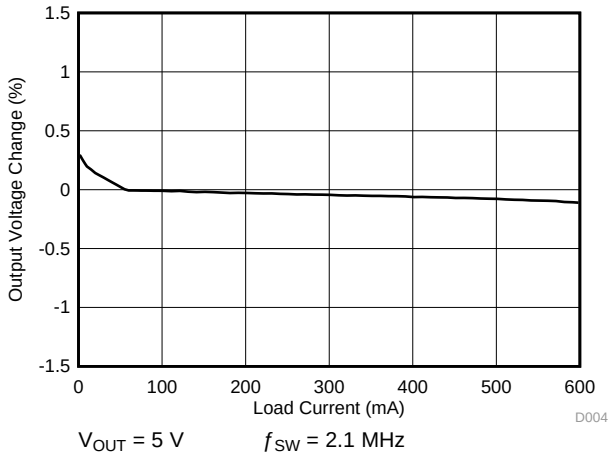
V_{OUT} = 12 V f_{SW} = 2100 kHz

Figure 1. Efficiency vs. Load Current



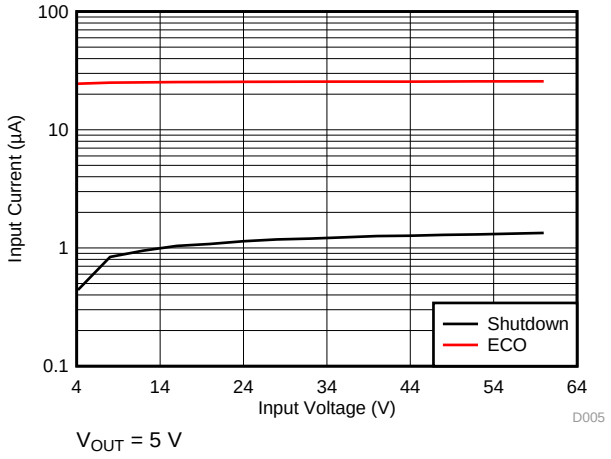
V_{OUT} = 5 V f_{SW} = 2100 kHz

Figure 2. Efficiency vs. Load Current



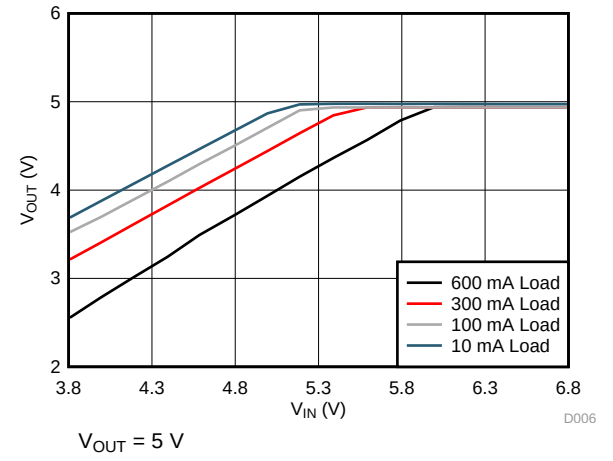
V_{OUT} = 5 V f_{SW} = 2.1 MHz

Figure 3. Load Regulation



V_{OUT} = 5 V

Figure 4. Shutdown Current and Quiescent Current



V_{OUT} = 5 V

Figure 5. Dropout Curve

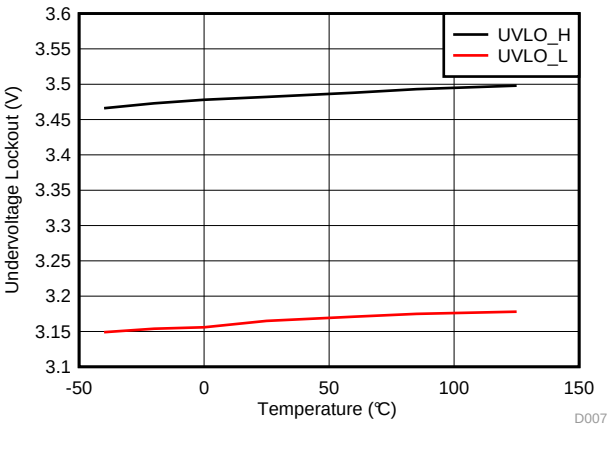


Figure 6. UVLO Threshold

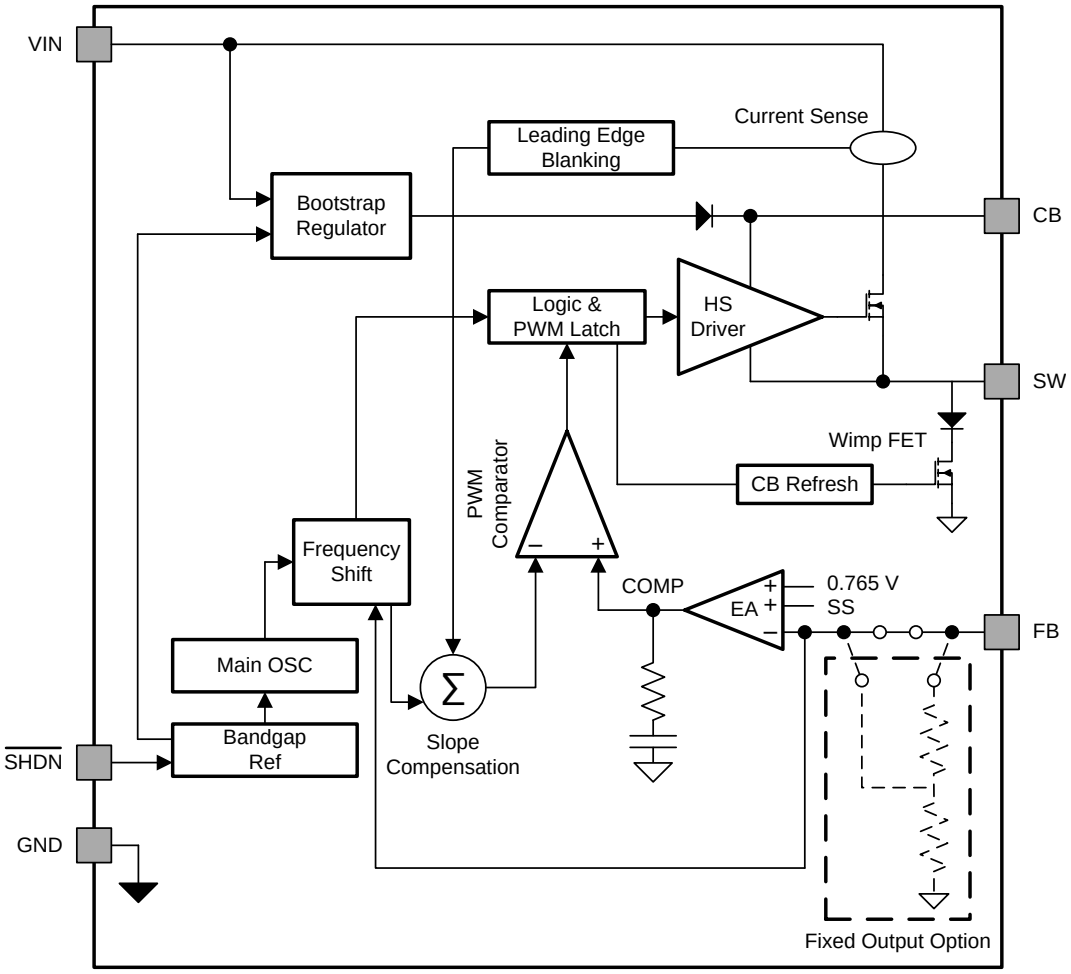
8 Detailed Description

8.1 Overview

The LMR16006Y-Q1 device is a 60 V, 600 mA, step-down (buck) regulator. The buck regulator has a very low quiescent current during light load to prolong battery life.

LMR16006Y-Q1 improves performance during line and load transients by implementing a constant frequency, current mode control which requires less output capacitance and simplifies frequency compensation design. The switching frequency is fixed at 2.1 MHz, thus smaller inductor and capacitor can be used. The device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the CB to SW pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The LMR16006Y-Q1 can operate at high duty cycles because of the boot UVLO and refresh the wimp FET. The output voltage can be stepped down to as low as the 0.8 V reference. Internal soft-start is featured to minimize inrush currents.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency PWM Control

The LMR16006Y-Q1 implements peak current mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier which drives the internal COMP node. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the level set by the internal COMP voltage, the power switch is turned off. The internal COMP node voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP node voltage to a maximum level.

8.3.2 Bootstrap Voltage (CB)

The LMR16006Y-Q1 has an integrated boot regulator, and requires a small ceramic capacitor between the CB and SW pins to provide the gate drive voltage for the high side MOSFET. The CB capacitor is refreshed when the high side MOSFET is off and the low side diode conducts. To improve drop out, the LMR16006Y-Q1 is designed to operate at 97% duty cycle as long as the CB to SW pin voltage is greater than 3 V. When the voltage from CB to SW drops below 3 V, the high side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the CB capacitor. Since the supply current sourced from the CB capacitor is low, the high side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high. Attention must be taken in maximum duty cycle applications with light load. To ensure SW can be pulled to ground to refresh the CB capacitor, an internal circuit will charge the CB capacitor when the load is light or the device is working in dropout condition.

8.3.3 Output Voltage Setting

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown on the front page schematic. The feedback pin voltage 0.765 V, so the ratio of the feedback resistors sets the output voltage according to the following equation: V_{OUT} = 0.765 V (1 + (R1/R2)). Typically R2 will be given as 1 kΩ to 100 kΩ for a starting value. To solve for R1 given R2 and V_{OUT} use R1 = R2 ((V_{OUT}/0.765 V) – 1).

8.3.4 Enable $\overline{\text{SHDN}}$ and VIN Undervoltage Lockout

LMR16006Y-Q1 $\overline{\text{SHDN}}$ pin is a high voltage tolerant input with an internal pull up circuit. The device can be enabled even if the $\overline{\text{SHDN}}$ pin is floating. The regulator can also be turned on using 1.23 V or higher logic signals. If the use of a higher voltage is desired due to system or other constraints, a 100 kΩ or larger resistor is recommended between the applied voltage and the $\overline{\text{SHDN}}$ pin to protect the device. When $\overline{\text{SHDN}}$ is pulled down to 0 V, the chip is turned off and enters the lowest shutdown current mode. In shutdown mode the supply current will be decreased to approximately 1 µA. If the shutdown function is not to be used the $\overline{\text{SHDN}}$ pin may be tied to V_{IN} via 100 kΩ resistor. The maximum voltage to the $\overline{\text{SHDN}}$ pin should not exceed 60 V. LMR16006Y-Q1 has an internal UVLO circuit to shutdown the output if the input voltage falls below an internally fixed UVLO threshold level. This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator will power up when the input voltage exceeds the voltage level. If there is a requirement for a higher UVLO voltage, the $\overline{\text{SHDN}}$ can be used to adjust the system UVLO by using external resistors.

8.3.5 Current Limit

The LMR16006Y-Q1 implements current mode control which uses the internal COMP voltage to turn off the high side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and internal COMP voltage are compared, when the peak switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP node high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

Feature Description (continued)

8.3.6 Overvoltage Transient Protection

The LMR16006Y-Q1 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low value output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will respond by clamping the error amplifier output to a high voltage. Thus, requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state duty cycle. In some applications, the power supply output voltage can respond faster than the error amplifier output can respond, this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot, when using a low value output capacitor, by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 108% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold, the high side MOSFET is allowed to turn on at the next clock cycle.

8.3.7 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C(typ). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160°C(typ), the device reinitiates the power up sequence.

8.4 Device Functional Modes

8.4.1 Continuous Conduction Mode

The LMR16006Y-Q1 steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at CCM), the buck regulator operates in two cycles. The power switch is connected between V_{IN} and SW. In the first cycle of operation the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by Cout and the rising current through the inductor. During the second cycle the transistor is open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as: $D = V_{OUT}/V_{IN}$ and $D' = (1-D)$ where D is the duty cycle of the switch, D and D' will be required for design calculations.

8.4.2 ECO Mode

The LMR16006Y-Q1 operates in ECO mode at light load currents to improve efficiency by reducing switching and gate drive losses. The LMR16006Y-Q1 is designed so that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the sleep current threshold, $I_{INDUCTOR} \leq 80$ mA, the device enters ECO mode. For ECO mode operation, the LMR16006Y-Q1 senses peak current, not average or load current, so the load current where the device enters ECO mode is dependent on V_{IN}, V_{OUT} and the output inductor value. When the load current is low and the output voltage is within regulation, the device enters an ECO mode and draws only 28 µA input quiescent current.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMR16006Y-Q1 is a step down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 600 mA. *Detailed Design Procedure* can be used to select components for the LMR16006Y-Q1.

9.2 Typical Application

Figure 7 shows typical application where user can adjust output by R1 and R2.

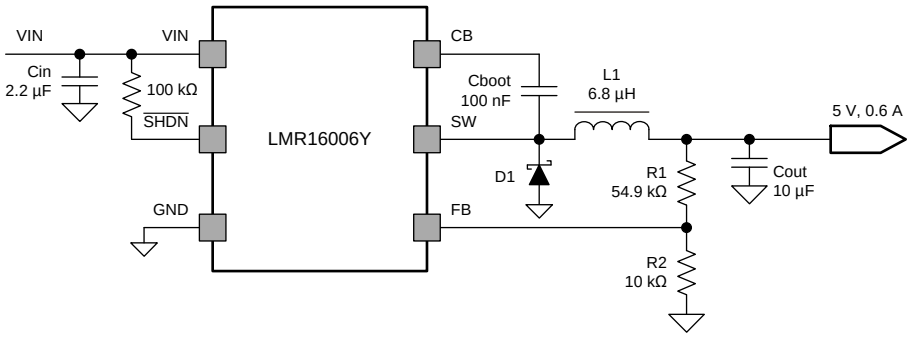


Figure 7. Application Circuit, 5 V Output

9.2.1 Design Requirements

Example requirements for typical buck regulators with high-efficiency applications:

Table 1. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
Input voltage, V_{IN}		9 V to 16 V, typical 12 V
Output voltage, V_{OUT}		5 V ± 3%
Maximum output current I_{O_max}		0.6 A
Minimum output current I_{O_min}		0.03 A
Transient response 0.03 A to 0.6 A		5%
Output voltage ripple		1%
Switching frequency f_{SW}		2.1 MHz
Target during Load Transient	Overvoltage peak value	106% of output voltage
	Undervoltage value	91% of output voltage

9.2.2 Detailed Design Procedure

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level:

9.2.2.1 Output Inductor Selection

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. To calculate the minimum value of the output inductor, use Equation 1. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. A reasonable value is setting the ripple current to be 30%-40% of the DC output current. For this design example, the minimum inductor value is calculated to be 6.82 µH, and a nearest standard value was chosen: 6.8 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 3 and Equation 4. The inductor ripple current is 0.074 A, and the RMS current is 0.60 A. As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. A good starting point for most applications is 6.8 µH with a 1.6 A current rating. Using a rating near 1.6 A will enable the LMR16006Y-Q1 to current limit without saturating the inductor. This is preferable to the LMR16006Y-Q1 going into thermal shutdown mode and the possibility of damaging the inductor if the output is shorted to ground or other long-term overload.

$$L_{o\,\min} = \frac{V_{in\max} - V_{out}}{I_o \times K_{IND}} \times \frac{V_{out}}{V_{in\max} \times f_{sw}} \quad (1)$$

$$I_{ripple} = \frac{V_{out} \times (V_{in\max} - V_{out})}{V_{in\max} \times L_o \times f_{sw}} \quad (2)$$

$$I_{L\text{-}RMS} = \sqrt{I_o^2 + \frac{1}{12} I_{ripple}^2} \quad (3)$$

$$I_{L-peak} = I_o + \frac{I_{ripple}}{2} \quad (4)$$

9.2.2.2 Output Capacitor Selection

The selection of Cout is mainly driven by three primary considerations. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 5 shows the minimum output capacitance necessary to accomplish this. The transient load response is specified as a 3% change in V_{OUT} for a load step from 0.03 A to 0.6 A (full load), $\Delta I_{OUT} = 0.6 – 0.03 = 0.57$ A and $\Delta V_{OUT} = 0.03 \times 5 = 0.15$ V. Using these numbers gives a minimum capacitance of 3.62 µF. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account.

The stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. Equation 6 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, Vf is the final peak output voltage, and Vi is the initial capacitor voltage. For this example, the worst case load step will be from 0.6 A to 0.03 A. The output voltage will increase during this load transition and the stated maximum in our specification is 3% of the output voltage. This will make Vo_overshoot = 1.03 × 5 = 5.15 V. V_i is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 6 yields a minimum capacitance of 1.6 µF.

Equation 7 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{sw} is the switching frequency, V_{o_ripple} is the maximum allowable output voltage ripple, and I_{L_ripple} is the inductor ripple current. Equation 7 yields 95 nF.

Equation 8 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 8 indicates the ESR should be less than 623 mΩ.

Additional capacitance de-ratings for aging, temperature and dc bias should be factored in which will increase this minimum value. For this example, 10 µF ceramic capacitors will be used. Capacitors in the range of 4.7 µF-100 µF are a good starting point with an ESR of 0.7 Ω or less.

$$C_{out} > \frac{2 \times \Delta I_{out}}{fsw \times \Delta V_{out}} \quad (5)$$

$$C_{out} > L_o \times \frac{(Ioh^2 - Iol^2)}{(Vf^2 - Vi^2)} \quad (6)$$

$$C_{out} > \frac{1}{8 \times fsw} \times \frac{1}{\frac{V_{o\_ripple}}{I_{L\_ripple}}} \quad (7)$$

$$R_{ESR} < \frac{V_{o\_ripple}}{I_{L\_ripple}} \quad (8)$$

9.2.2.3 Schottky Diode Selection

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. In the target application, the current rating for the diode should be equal or greater to the maximum output current for best reliability in most applications. In cases where the input voltage is not much greater than the output voltage the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately (1-D) × I_{OUT}. However the peak current rating should be higher than the maximum load current. A 0.5 A to 1 A rated diode is a good starting point.

9.2.2.4 Input Capacitor Selection

A low ESR ceramic capacitor is needed between the VIN pin and ground pin. This capacitor prevents large switching voltage transients from appearing at the input. Use a 1 µF-10 µF value with X5R or X7R dielectric. Depending on construction, a ceramic capacitor's value can decrease up to 50% of its nominal value when rated voltage is applied. Consult with the capacitor manufactures data sheet for information on capacitor derating over voltage and temperature. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the LMR16006Y-Q1. The input ripple current can be calculated using below Equation 9.

For this example design, one 2.2 µF, 50 V capacitor is selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 10. Using the design example values, I_{OUT_max} = 0.6 A, Cin = 2.2 µF, f_{SW} = 2100 kHz, yields an input voltage ripple of 33 mV and a rms input ripple current of 0.3 A.

$$I_{cirms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{in\,\min}} \times \frac{(V_{in\,\min} - V_{out})}{V_{in\,\min}}} \quad (9)$$

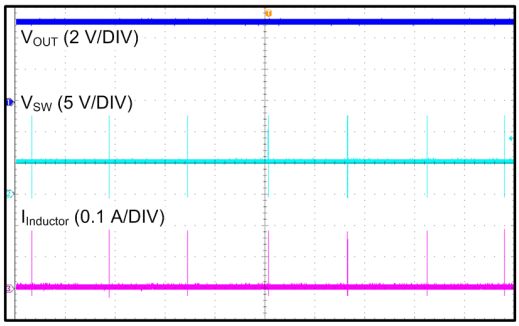
$$\Delta V_{in} = \frac{I_{out\,\max} \times 0.25}{C_{in} \times fsw} \quad (10)$$

9.2.2.5 Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitor or larger is recommended for the bootstrap capacitor (C_{BOOT}). For applications where the input voltage is close to output voltage a larger capacitor is recommended, generally 0.1 µF to 1 µF to ensure plenty of gate drive for the internal switches and a consistently low R_{DSON}. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

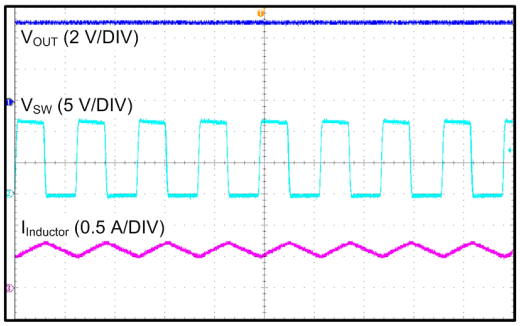
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 2100 kHz, L1 = 6.8 µH, C_{OUT} = 10 µF, T_A = 25°C.



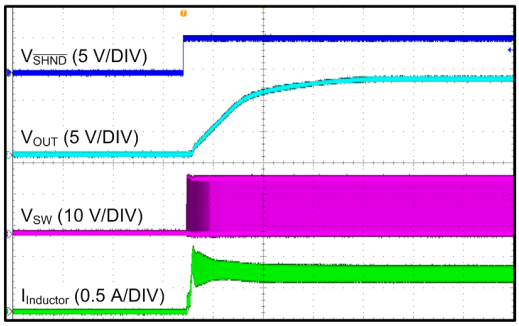
V_{OUT} = 5 V I_{OUT} = 0 mA

Figure 8. Steady State Waveform



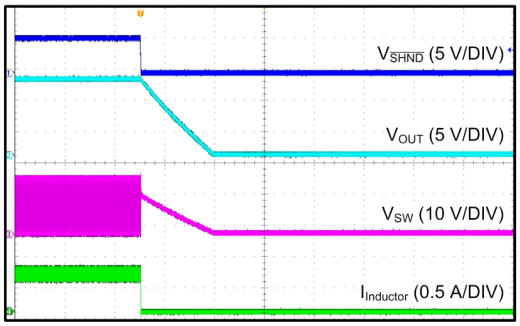
V_{OUT} = 5 V I_{OUT} = 600 mA

Figure 9. Steady State Waveform



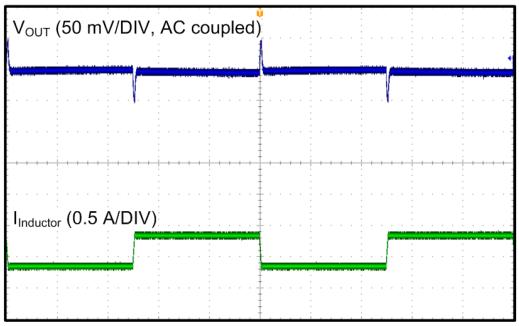
V_{IN} = 15 V V_{OUT} = 12 V I_{OUT} = 600 mA

Figure 10. Start-Up



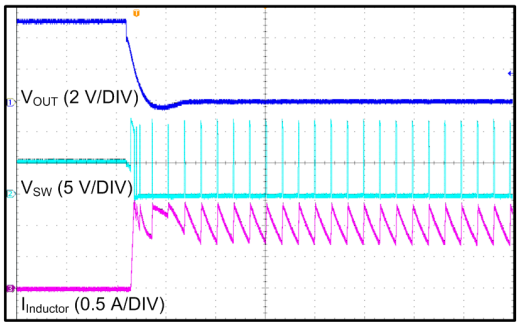
V_{IN} = 15 V V_{OUT} = 12 V I_{OUT} = 600 mA

Figure 11. Shutdown



V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 600 mA

Figure 12. Load Transient from 0.1 A to 0.6 A



V_{IN} = 12 V V_{OUT} = 5 V

Figure 13. Short Circuit Entry

9.2.4 Additional Application Circuit

Figure 14 shows the typical application circuit with a fixed output.

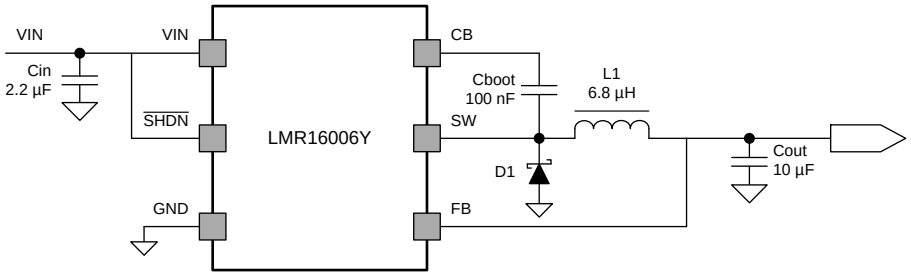


Figure 14. LMR16006Y-Q1 Application Circuit, Fixed Output

10 Power Supply Recommendations

The LMR16006Y-Q1 is designed to operate from an input voltage supply range between 4 V and 60 V. This input supply should be able to withstand the maximum input current and maintain a voltage above 4 V. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMR16006Y-Q1 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR16006Y-Q1, additional bulk capacitance may be required in addition to the ceramic input capacitors.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor to minimize coupling noise into the feedback pin.
2. The input bypass capacitor Cin must be placed close to the V_{IN} pin. This will reduce copper trace resistance which effects input voltage ripple of the IC.
3. The inductor L1 should be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor, Cout should be placed close to the junction of L1 and the diode D1. The L1, D1, and Cout trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.
5. The ground connection for the diode, Cin, and Cout should be as small as possible and tied to the system ground plane in only one spot (preferably at the Cout ground point) to minimize conducted noise in the system ground plane.
6. For more detail on switching power supply layout considerations see AN-1149 *Layout Guidelines for Switching Power Supplies* SNVA021

11.2 Layout Example

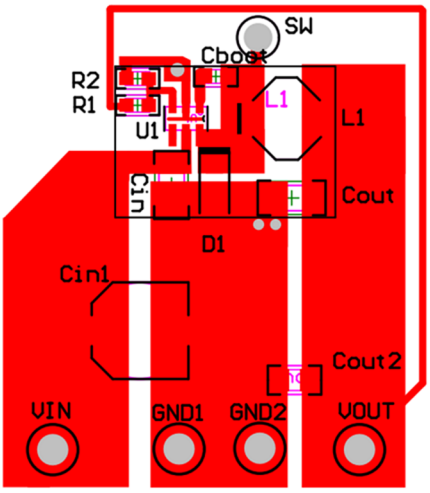


Figure 15. Layout

12 Device and Documentation Support

12.1 Related Documentation

AN-1149 *Layout Guidelines for Switching Power Supplies* (SNVA021).

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
SIMPLE SWITCHER is a registered trademark of TI .
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR16006YQ3DDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q32Y	Samples
LMR16006YQ3DDCTQ1	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q32Y	Samples
LMR16006YQ5DDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q52Y	Samples
LMR16006YQ5DDCTQ1	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q52Y	Samples
LMR16006YQDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q02Y	Samples
LMR16006YQDDCTQ1	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q02Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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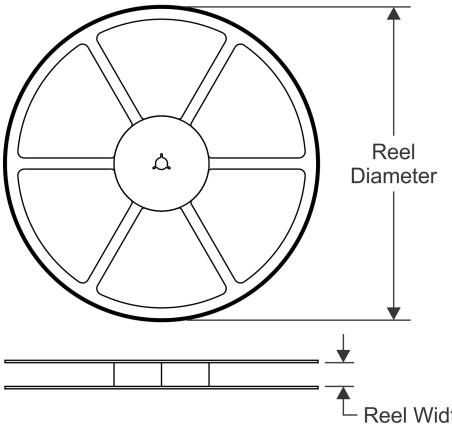
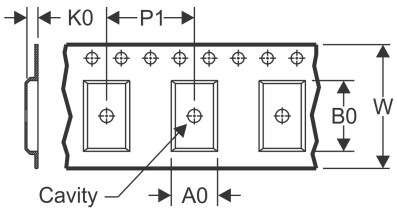
TAPE AND REEL INFORMATION

REEL DIMENSIONS

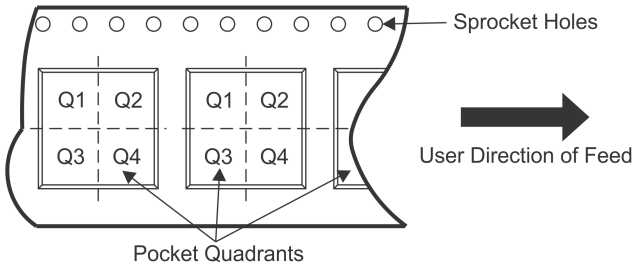


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

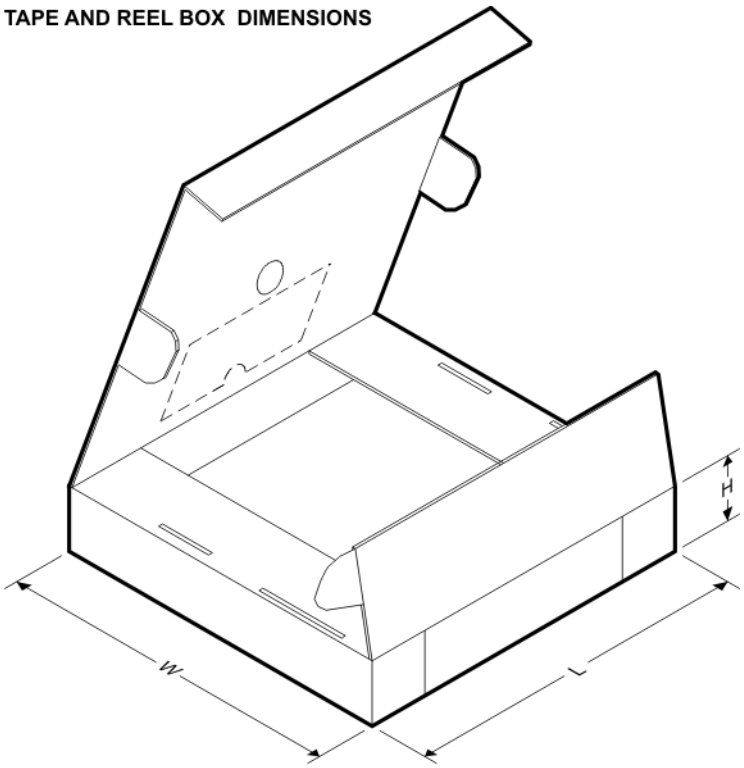
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR16006YQ3DDCRQ1	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR16006YQ3DDCTQ1	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR16006YQ5DDCRQ1	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR16006YQ5DDCTQ1	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR16006YQDDCRQ1	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMR16006YQDDCTQ1	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

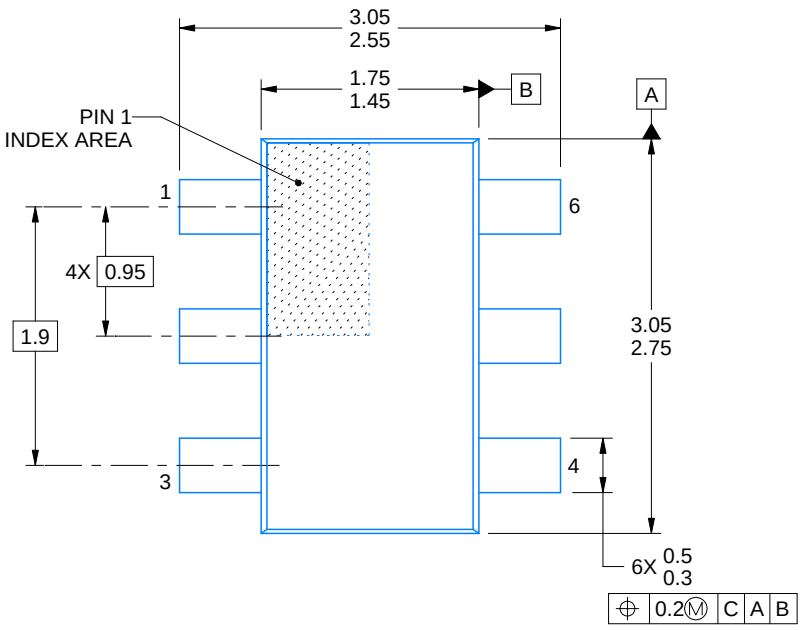
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR16006YQ3DDCRQ1	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMR16006YQ3DDCTQ1	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
LMR16006YQ5DDCRQ1	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMR16006YQ5DDCTQ1	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
LMR16006YQDDCRQ1	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LMR16006YQDDCTQ1	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0

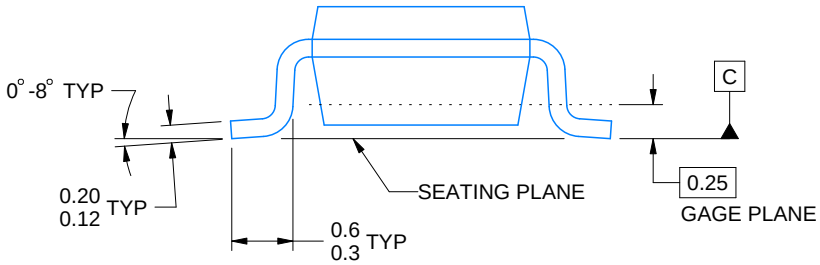
PACKAGE OUTLINE

DDC0006A

SOT - 1.1 max height

SOT





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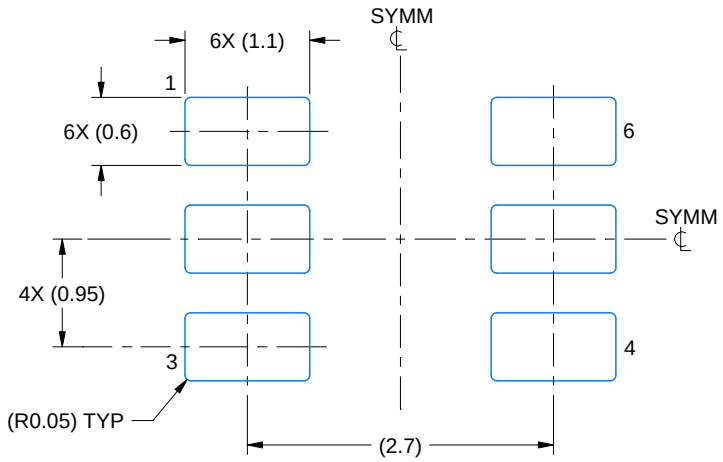
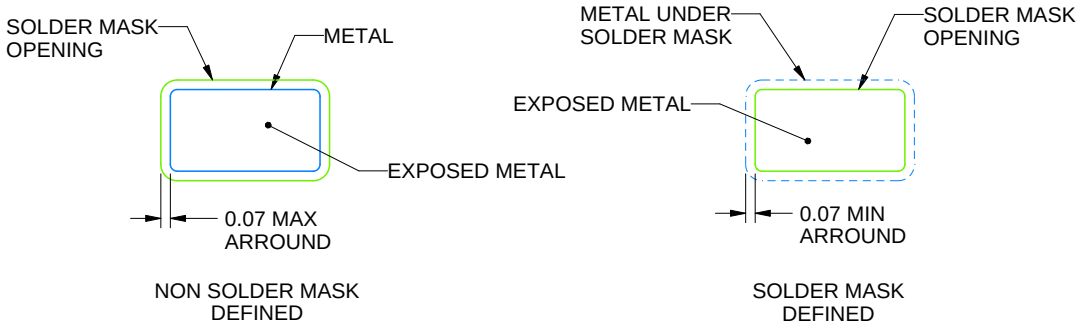
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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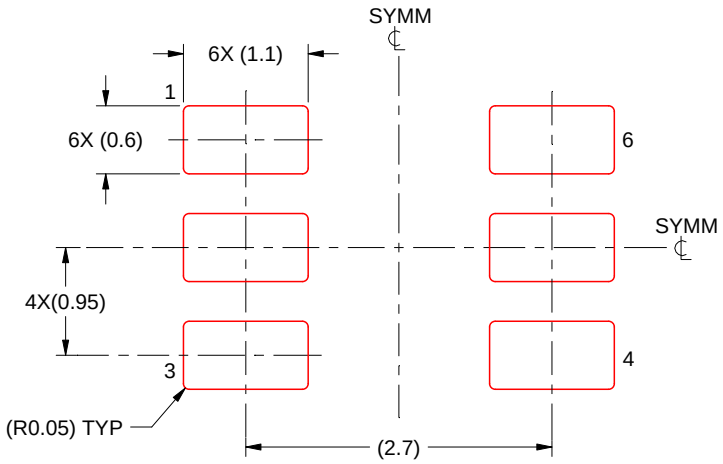
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/B 11/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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