Applications Note: AN_SY7080

0.9V Minimum Input and 4V Maximum Output 0.8A Peak Current Synchronous Boost with Output Disconnect

Preliminary Specification

General Description

SY7080 is a high efficiency synchronous boost regulator that converts down to 0.9V input into up to 4V output voltage. It adopts N-MOS for the main switch and P-MOS for the synchronous switch. It can disconnect the output during the shutdown operation.

Features

- 0.9V to 4V wide input range
- 4V max output voltage
- 1.2MHz switching frequency
- Minimum on time: 80ns typical
- Minimum off time: 60ns typical
- Output disconnect at shutdown
- Low $R_{DS(ON)}$ (main switch/synchronous switch) at 3.3V output: 90/200mΩ
- Compact SOT23-6

Ordering Information

SY7080□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Note
SY7080ABC	SOT23-6	----

Applications

- LiIon or LiPolymer powered Cell Phones, DSCs, PMP, GPS.
- Alkaline battery powered electronic equipment.
- wireless mouse.

Typical Applications

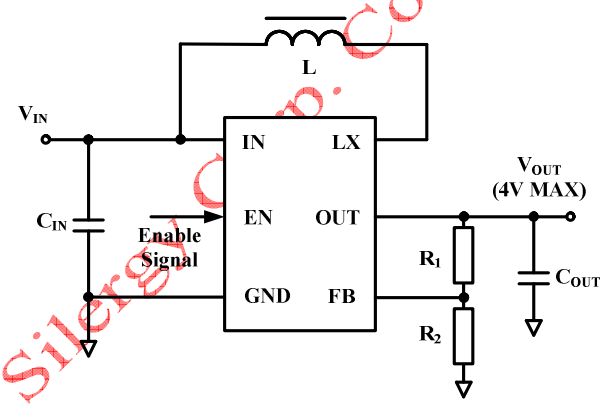


Figure 1. Schematic Diagram

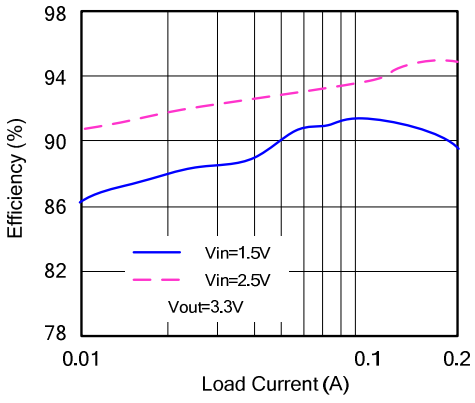
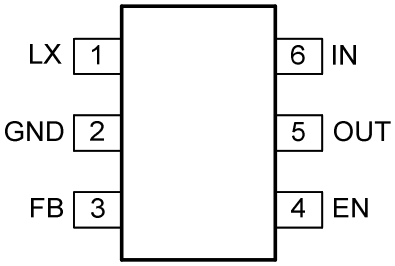


Figure 2. Efficiency vs Load Current

Pinout (top view)



(SOT23-6)

Top mark: **EE*xyz*** (Device code:EE., ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN	6	Input pin. Decouple this pin to GND pin with 1uF ceramic cap
GND	2	Ground pin
EN	4	Enable pin. Apply a voltage higher than 0.9V to turn on the part. Pull it low or leave it open to shut down the part.
OUT	5	Output pin. Decouple this pin to GND pin with a minimum of 22uF ceramic cap
LX	1	Inductor node. Connect an inductor between IN pin and LX pin
FB	3	Feedback pin. Connect a resistor R_1 between OUT and FB, and a resistor R_2 between FB and GND to program the output voltage. V_{OUT}=1.2V*(R_1/R_2+1)

Absolute Maximum Ratings (Note 1)

All Pins to GND---------- 4.5V
Power Dissipation, P_D @ T_A = 25°C SOT23-6 ---------- 0.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 161°C/W
θ_{JC} ---------- 130°C/W
Junction Temperature Range ---------- 125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility (Note 2)
HBM (Human Body Mode) ----------2kV
MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

IN ---------- 0.9V to 4V
EN ---------- 0V to V_{OUT}+0.3V
All other pins ---------- 0-4V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =2.5V, V_{OUT}=3.3V, I_{OUT}=100mA, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Input Voltage	V_{IN}	R_{LOAD}=2kΩ		0.9		V
Output Voltage Range	V_{OUT}		2.5		4	V
Quiescent Current	I_Q	EN=high, V_{FB}=1.32V		65		μA
Shutdown Current	I_{SHDN}	EN=0V			1	μA
EN Rising Threshold	V_{ENH}		0.9			V
EN Falling Threshold	V_{ENL}				0.4	V
Low Side Main FET R_{ON}	$R_{DS(ON)1}$			90		mΩ
Synchronous FET R_{ON}	$R_{DS(ON)2}$			200		mΩ
Main FET Current Limit	I_{LIM1}			1.8		A
Switching Frequency	Fsw		1.0	1.2	1.4	MHz
Feedback Reference Voltage	V_{REF}		1.164	1.2	1.236	V
Thermal Shutdown Temperature	T_{SD}			150		℃

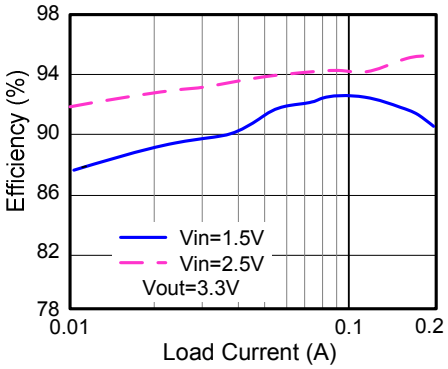
Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

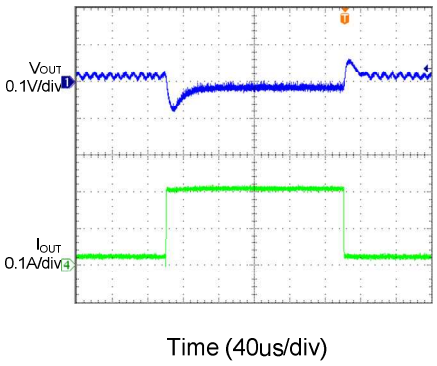
Typical Performance Characteristics

Efficiency vs Load Current



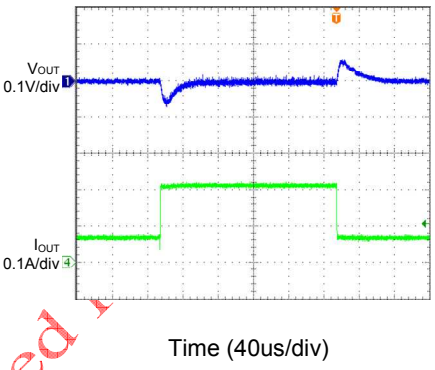
Load Transient

(VIN=1.5V, VOUT=3.3V, Iload=0.03-0.2A)



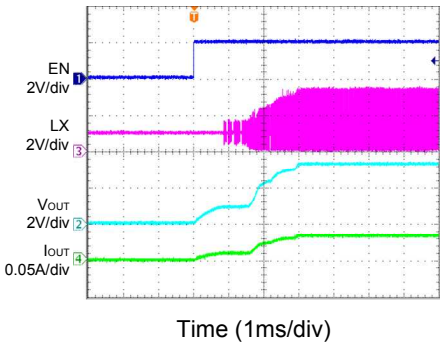
Load Transient

(VIN=1.5V, VOUT=3.3V, Iload=0.06-0.2A)



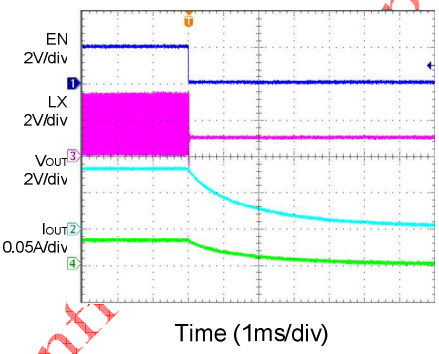
Startup from Enable

(VIN=0.9V, VOUT=3.3V, Rload=100Ω)



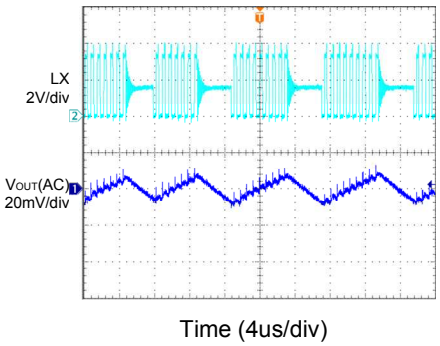
Shutdown from Enable

(VIN=0.9V, VOUT=3.3V, Rload=100Ω)



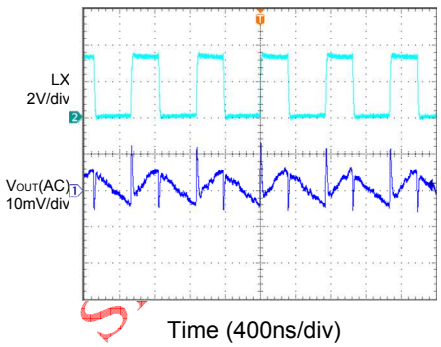
Output Ripple

(VIN=1.5V, VOUT=3.3V, Iload=30mA)



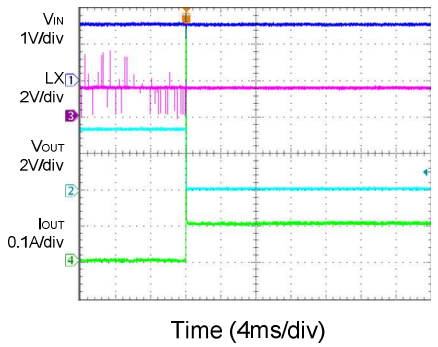
Output Ripple

(VIN=1.5V, VOUT=3.3V, Iload=200mA)



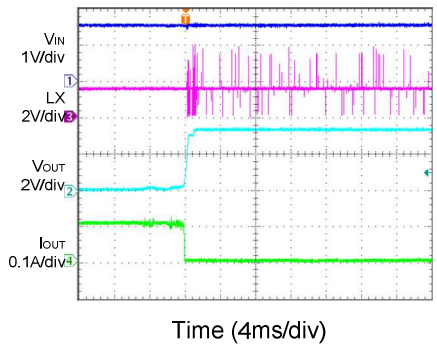
Open Load to Short

(VIN=1.5V, VOUT=3.3V)



Short Recovery

(VIN=1.5V, VOUT=3.3V)



Applications Information

Because of the high integration in the SY7080 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10k and 1M is recommended for both resistors. If R_2=120k is chosen, then R_1 can be calculated to be:

$$R_1 = \frac{(V_{OUT} - 1.2V) \times R_2}{1.2V}$$

Input capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}$$

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor with 6.3V rating and greater than 20uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.
The SY7080 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{IN}}{V_{OUT}}\right) \times I_{OUT,MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Layout Design:

The layout design of SY7080 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

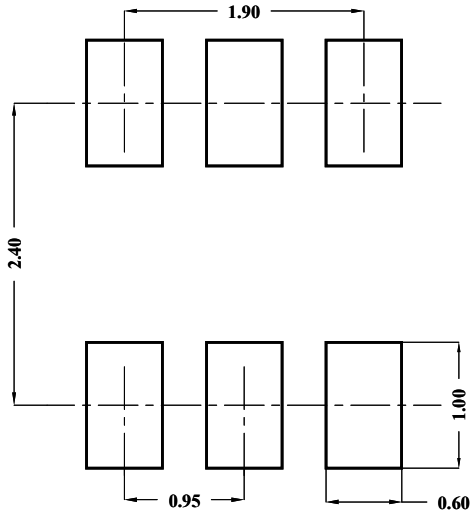
2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

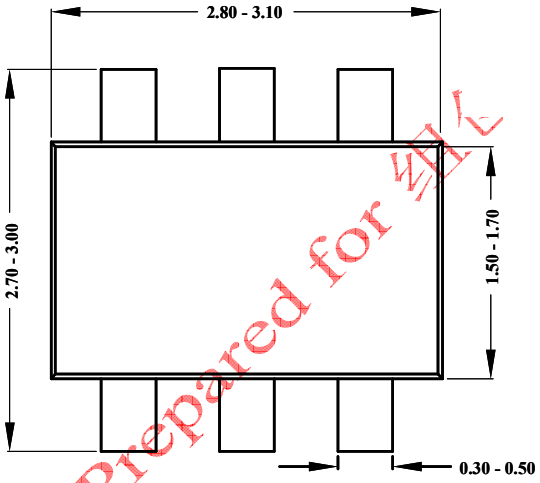
4) The components R_1 and R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

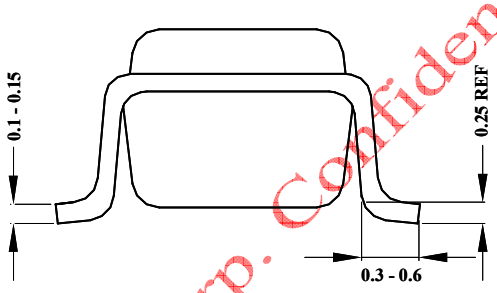
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

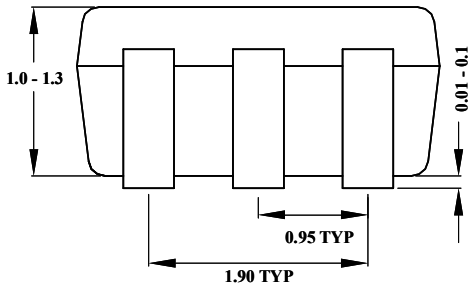
SOT23-6 Package outline & PCB layout design



Recommended Pad Layout







Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.