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CCD linear image sensor

S12379

Pixel size: 8 × 8 µm, 4-port readout, front-illuminated CCD with high-speed response and high sensitivity

The S12379 is a high-speed line rate, front-illuminated CCD linear image sensor designed for machine vision cameras.

Features

- **Pixel size: 8 × 8 µm**
- **2048 pixels**
- **High-speed multiport readout (Readout speed: 40 MHz max. × 4 ports)**
- **High CCD node sensitivity: 21 µV/e^- typ.**
- **Anti-blooming function**

Application

- **Machine vision**
- **High-speed image readout**

Structure

Parameter	Specification	Unit
Image size (H × V)	16.384 × 0.008	mm
Pixel size (H × V)	8 × 8	µm
Total number of pixels	2104	-
Number of effective pixels	2048	-
Fill factor	100	%
Horizontal clock	2-phase	-
Output circuit	3-stage MOSFET source follower	-
Package	24-pin ceramic DIP	-
Window material	Quartz glass*1	

*1: Resin sealing

Absolute maximum ratings (Ta=25 °C, unless otherwise noted)

Parameter	Symbol	Condition	Value	Unit
Operating temperature	Topr	Package temperature, no dew condensation*2	-50 to +70	°C
Storage temperature	Tstg	No dew condensation*2	-50 to +70	°C
Output transistor drain voltage	$V_{OD1, 2, 3, 4}$		-0.5 to +20	V
Reset drain voltage	V_{RD}		-0.5 to +18	V
Anti-blooming drain voltage	V_{ABD}		-0.5 to +18	V
Anti-blooming gate voltage	V_{ABG}		-0.5 to +15	V
Storage gate voltage	V_{STG}		-0.5 to +15	V
Transfer gate voltage	V_{TG}		-0.5 to +15	V
Reset gate voltage	V_{RG12}, V_{RG34}		-0.5 to +15	V
Output gate voltage	V_{OG}		-0.5 to +15	V
Horizontal shift register clock voltage	V_{P1H}, V_{P2H}		-0.5 to +15	V

*2: When there is a temperature difference between a product and the surrounding area in high humidity environment, dew condensation may occur on the product surface. Dew condensation on the product may cause deterioration in characteristics and reliability.

Note: Exceeding the absolute maximum ratings even momentarily may cause a drop in product quality. Always be sure to use the product within the absolute maximum ratings.
The sensor temperature will increase during high-speed operation. Take heat dissipation measures as required to prevent exceeding the absolute maximum ratings.

Operating conditions (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		$V_{OD1, 2, 3, 4}$	13	15	17	V
Reset drain voltage		V_{RD}	12	13	14	V
Anti-blooming drain voltage		V_{ABD}	12	13	14	V
Anti-blooming gate voltage		V_{ABG}	0	0	5	V
Storage gate voltage		V_{STG}	0	0	5	V
Transfer gate voltage	High	V_{TGH}	8	10	12	V
	Low	V_{TGL}	0	0	3	
Reset gate voltage	High	V_{RG12H}, V_{RG34H}	7	8	9	V
	Low	V_{RG12L}, V_{RG34L}	0	0	1	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	5.5	6	6.5	V
	Low	V_{P1HL}, V_{P2HL}	0	0	1	
Output gate voltage		V_{OG}	6	7	8	V
Substrate voltage		V_{SS}	-	0	-	V
External load resistance		R_L	2.0	2.2	2.4	kΩ

Electrical characteristics (Ta=25 °C, operating conditions: Typ., unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output signal frequency/port	fc	-	20	40	MHz
Line rate	LR	-	36	72	kHz
Reset clock frequency	frg	-	20	40	MHz
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	180	-	pF
Transfer gate capacitance	C_{TG}	-	110	-	pF
Reset gate capacitance	C_{RG12}, C_{RG34}	-	20	-	pF
Charge transfer efficiency*3	CTE	0.99995	0.99999	-	-
DC output level*4	Vout	8	9	10	V
Output impedance*4	Zo	-	135	200	Ω
Power consumption/port*4 *5	P	-	100	140	mW

*3: Transfer efficiency per CCD shift register pixel measured at half the saturation output
*4: Varies depending on the load resistance (V_{OD}=15 V, load resistance=2.2 kΩ)
*5: Power consumption of the on-chip amp and load resistance

Electrical and optical characteristics (Ta=25 °C, operating conditions: Typ., unless otherwise noted)

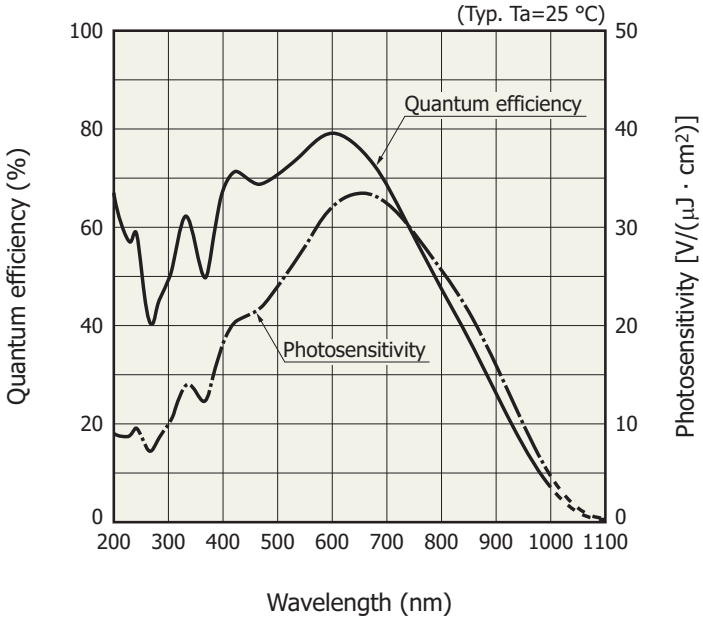
Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × Sv	-	V
Saturation charge*6		Fw	15	20	-	ke^-
CCD node sensitivity		Sv	19	21	23	$\mu V/e^-$
Dark current*7	Average of all effective pixels	DSave	-	30	100	e^-/ms
	Maximum among all effective pixels	DSmax	-	40	100	
Readout noise*8		Nr	-	20	30	e^- rms
Dynamic range*9		DR	600	1000	-	-
Spectral response range		λ	-	200 to 1000	-	nm
Photoresponse nonuniformity*10 *11		PRNU	-	±3	±10	%
Image lag*10 *12		L	-	0.1	1	%

*6: Saturation charge is within linearity ± 2%.
*7: Dark current is halved when cooled by 5 to 7 °C.
*8: Readout frequency 40 MHz
*9: Dynamic range = saturation charge/readout noise
*10: Measured at half the saturation output using an LED light (peak emission wavelength: 470 nm)

*11: Photoresponse nonuniformity = $\frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$ [%]

*12: Percentage of unread signal level when a light pulse is directed so that the output is half the saturation output

Spectral response (without window)



* Spectral response will degrade depending on the transmittance of the quartz glass.

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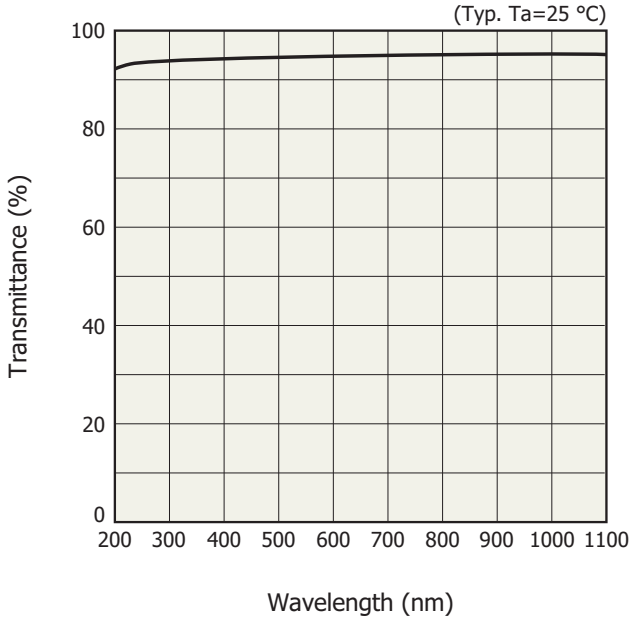
Spectral transmittance of window material



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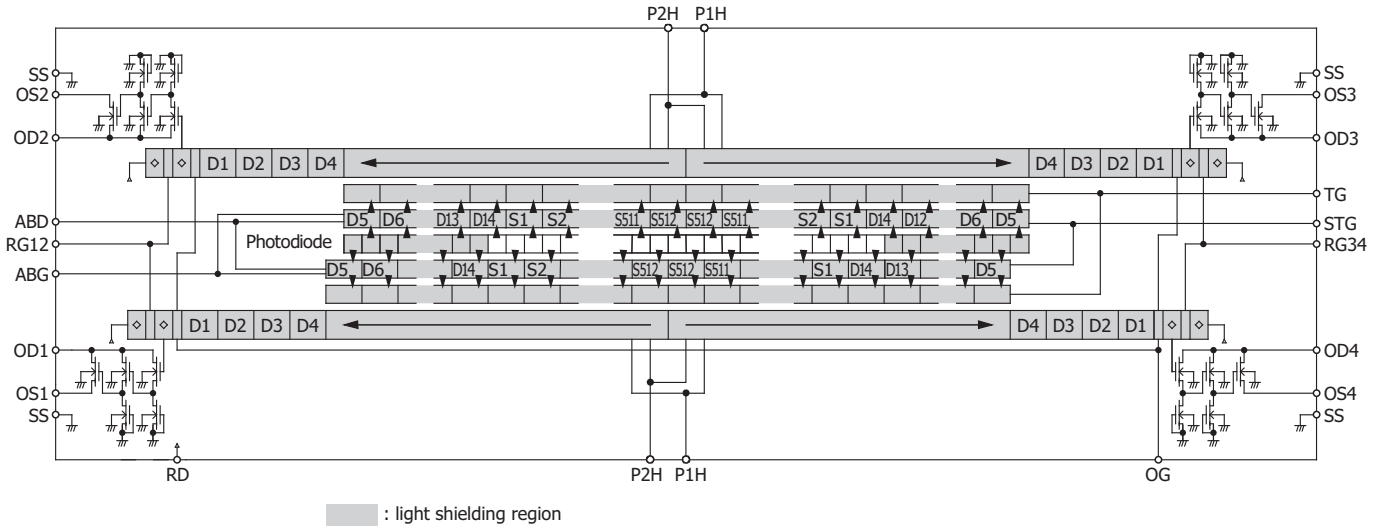
Device structure (schematic of CCD chip as viewed from top of dimensional outline)



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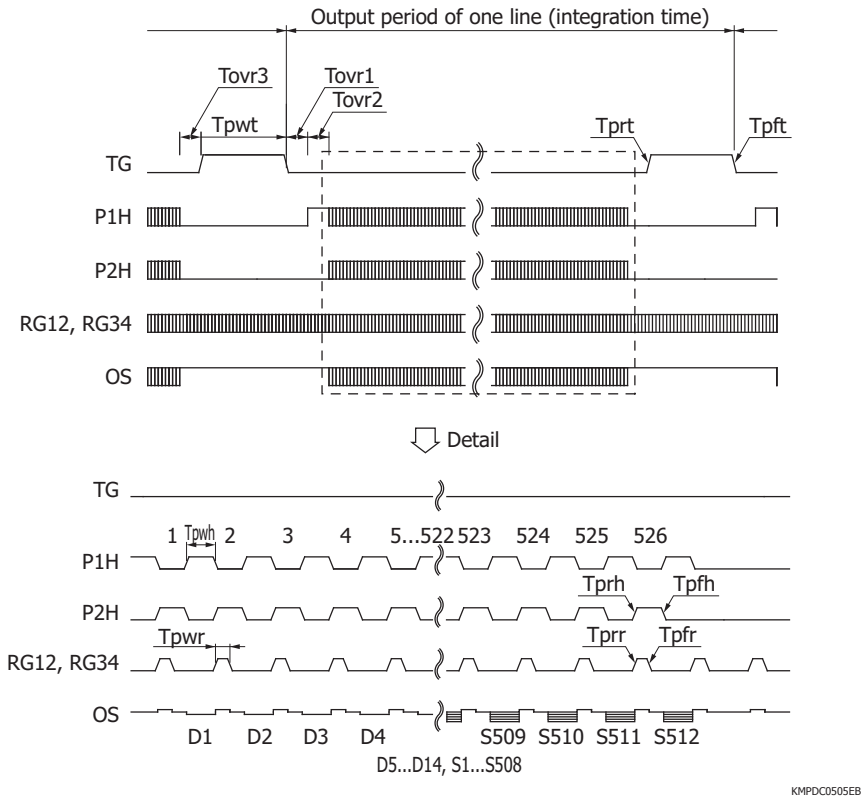
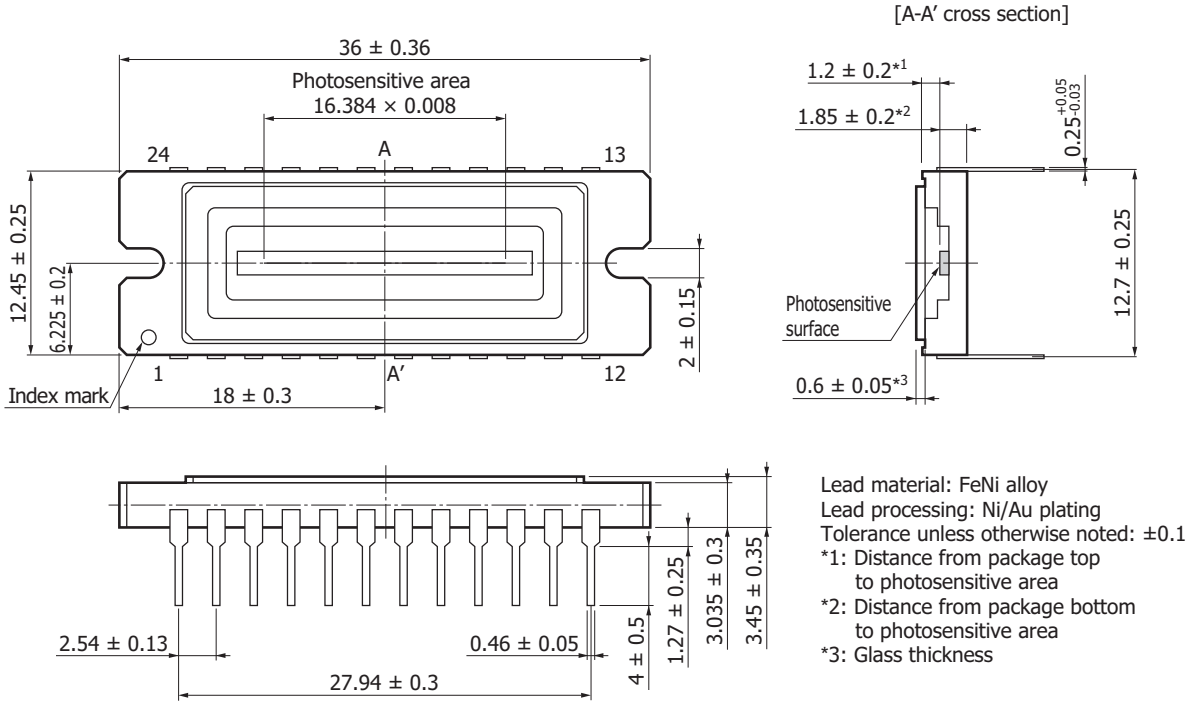
Timing chart



Parameter		Symbol	Min.	Typ.	Max.	Unit
TG	Pulse width	Tpwt	400	600	-	ns
	Rise and fall times	Tprt, Tpft	10	-	-	ns
P1H, P2H *12	Pulse width	Tpwh	12.5	25	-	ns
	Rise and fall times	Tprh, Tpfh	6	-	-	ns
	Duty ratio	-	40	50	60	%
RG12, RG34	Pulse width	Tpwr	5	6	-	ns
	Rise and fall times	Tprr, Tpfr	2	-	-	ns
TG-P1H	Overlap time	Tovr1	100	200	-	ns
		Tovr2	100	200	-	ns
		Tovr3	100	200	-	ns

*12: Symmetrical clock pulses should be overlapped at 50% of maximum pulse amplitude.

Dimensional outline (unit: mm)



Lead material: FeNi alloy
Lead processing: Ni/Au plating
Tolerance unless otherwise noted: ±0.1
*1: Distance from package top to photosensitive area
*2: Distance from package bottom to photosensitive area
*3: Glass thickness

Note: This product is not hermetically sealed, and therefore moisture may permeate into the package. Storing or using the product in a place with sudden temperature or humidity changes may cause condensation to form inside the package, so avoid such locations.

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Pin connections

Pin no.	Symbol	Function	Remark (standard operation)
1	SS	Substrate	0 V
2	OS1	Output transistor source 1	RL=2.2 kΩ (OS1-SS)
3	OD1	Output transistor drain 1	+15 V
4	RD	Reset drain	+13 V
5	ABG	Anti-blooming gate	0 V
6	P2H	Horizontal shift register clock 2	+6/0 V
7	P1H	Horizontal shift register clock 1	+6/0 V
8	RG12	Reset gate 1, 2	+8/0 V
9	OG	Output gate	+7 V
10	OD4	Output transistor drain 4	+15 V
11	OS4	Output transistor source 4	RL=2.2 kΩ (OS4-SS)
12	SS	Substrate	0 V
13	SS	Substrate	0 V
14	OS3	Output transistor source 3	RL=2.2 kΩ (OS3-SS)
15	OD3	Output transistor drain 3	+15 V
16	STG	Storage gate	0 V
17	RG34	Reset gate 3, 4	+8/0 V
18	P1H	Horizontal shift register clock 1	+6/0 V
19	P2H	Horizontal shift register clock 2	+6/0 V
20	TG	Transfer gate	+10/0 V
21	ABD	Anti-blooming drain	+13 V
22	OD2	Output transistor drain	+15 V
23	OS2	Output transistor source 2	RL=2.2 kΩ (OS2-SS)
24	SS	Substrate	0 V

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

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